Rockwell Automation
Allen-Bradley

Bulletin 1402
Line Synchronization Module (LSM)

Application Notes

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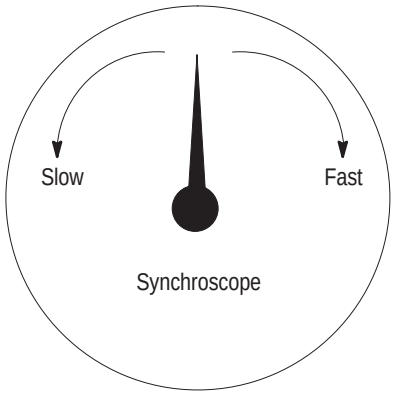
What is Synchronization?

Synchronous generators, or alternators, are the primary energy conversion devices of the world's electric power systems today. Alternators are usually not used solely to supply individual loads. Alternators are connected to a power supply system known as a bus. Alternators connected to a bus are used as auxiliary power sources and as available stand-by power sources. Depending on the power demand on the system as a whole, alternators may be connected or disconnected from a main power bus or from a utility feed distribution bus. The process of connecting an alternator to a system bus is called *paralleling* with the system bus, or **synchronization.** Before an alternator may be connected with a main power bus, the incoming alternator and the main power bus must have the same:

- RMS Voltage
- Frequency
- Phase Displacement

One standard method of monitoring the condition of the alternator bus frequency and phase, relative to the rest of the system, is through the use of a synchroscope.

Figure 1
Synchroscope

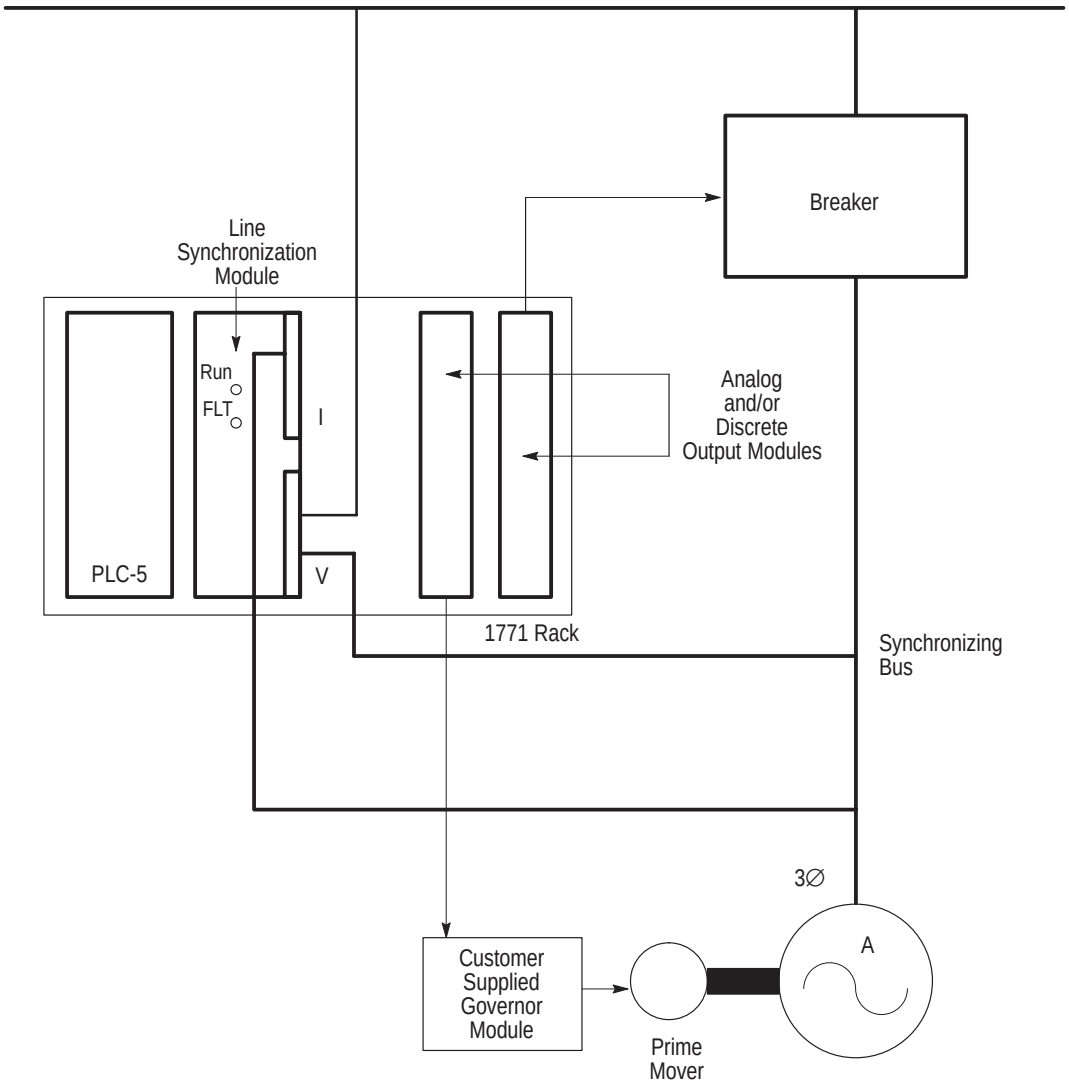


The position of the needle indicates the phase difference between the voltages of the incoming alternator and the main power bus. When the needle is pointed straight up as pictured, there is no phase difference between the two busses. While the rate of motion of the needle indicates frequency difference, the direction of motion of the needle indicates that the frequency of the incoming alternator is higher or lower than the main power bus. When the frequency or the phase of the two busses are different, the speed of the alternator may be appropriately adjusted through the power supplied to the prime mover. Correcting for frequency differences between the two busses may be viewed as *coarse* speed adjustments while correcting for phase differences may be viewed as *fine* speed adjustments. When the synchroscope needle remains at or moves slowly past the point of 0° phase difference, the frequency and phase of the two busses match. If the RMS voltage levels of the two busses are the same at this point, the breaker that connects the two busses may be closed.

Synchronization

The LSM provides an extremely accurate and quick means of monitoring all synchronization parameters, completing synchronization more quickly, more repeatably, and more efficiently than ever previously possible.

Figure 2
Utility Feed (Reference Bus) 3∅



The following pages contain several LSM application sample ladder programs. **No warranty is expressed or implied by using these ladder programs.** Each of the ladders listed is subject to change. It is assumed that prior to running any of the programs listed in this document, the configuration ladder program located in Appendix C of Publication 1402-5.0, *LSM Installation and Operation Manual* has been successfully completed.

Because the synchronization process is application specific, existing parameters in this document may require alteration for particular applications. The outputs in the listed sample programs are based on raw D/A counts. Differing installations may require different output methods.

1771 Modules and Rack Locations

The sample ladder logic programs were written using the following Allen-Bradley 1771 modules in the rack locations specified.

Rack/Group	Cat. No.	Description
0/0	1771-IAD	120V AC/DC Input Module
0/1	1771-OAD	12V to 120V AC Output Module
0/2	1402-LS51	Line Synchronization Module
0/4	1771-OFE1	Analog Output Module
0/5	1771-SIM	I/O Simulator Module

Synchronization Utilizing the 6200 PID Instruction

PID (Proportional, Integral, Derivative)

PID Background

PID compensating is a method used to correct system error. PID compensation is commonly used in feedback control systems. A PID controller can be viewed as giving control that is a function of past trending, present, and predicted future error of a system.

$$m(t) = K_p e(t) + K_1 \int e(t)dt + K_D \frac{de(t)}{dt}$$

m(t) = Corrected system output
e(t) = System error as a function of time

Proportional Term K_P

The role of the Proportional term in the PID process is to compensate for immediate changes in error. The proportional term provides for the system output a component that is a function of the present error of the system. The error value is amplified by a constant amount, and the system output is appropriately compensated. The proportional compensation component only uses the present error; time is not a factor in proportional control.

Integral Term K_I

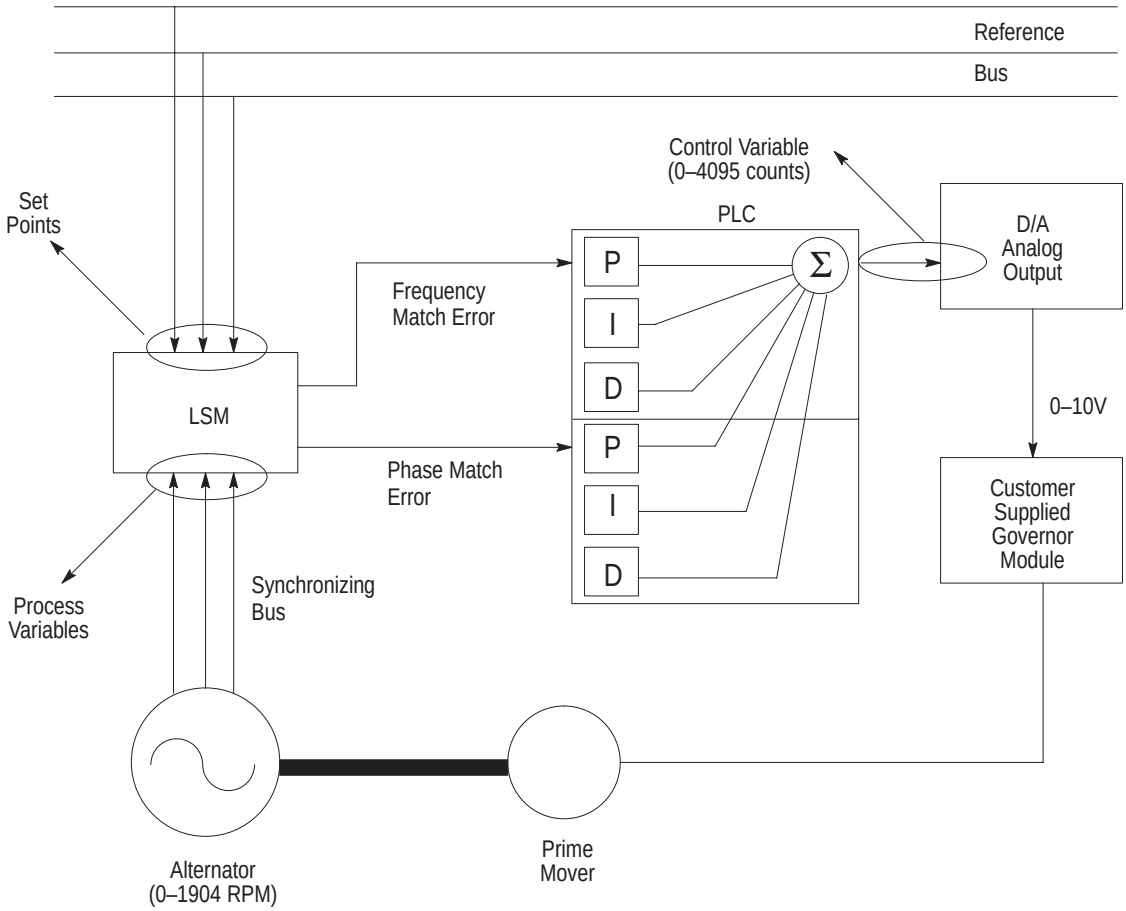
The Integral term compensates for system error by accumulating error corrections over time. If applied to a system with steady state error, the Integral term will accumulate this constant error over a certain calculation period. The output from the Integral component then will be quite large. To avoid highly under damped control output, the calculation period and the Integral term must be appropriately set. The Integration compensation component is useful for long term correction, such as motor loading.

Derivative Term K_D

The Derivative term compensates system output by *anticipating* system error. The Derivative term utilizes the values of the change in system error over a derivative update period and the actual length of the update period. By measuring the rate of change of system error, the derivative term observes trends in error. The compensated system output as a result of the Derivative term is the difference in error from one period to the next multiplied by the Derivative term.

The listed PID methods can be implemented using the PID control instruction of the Allen-Bradley PLC-5® family of processors.

Figure 3
PID Synchronization



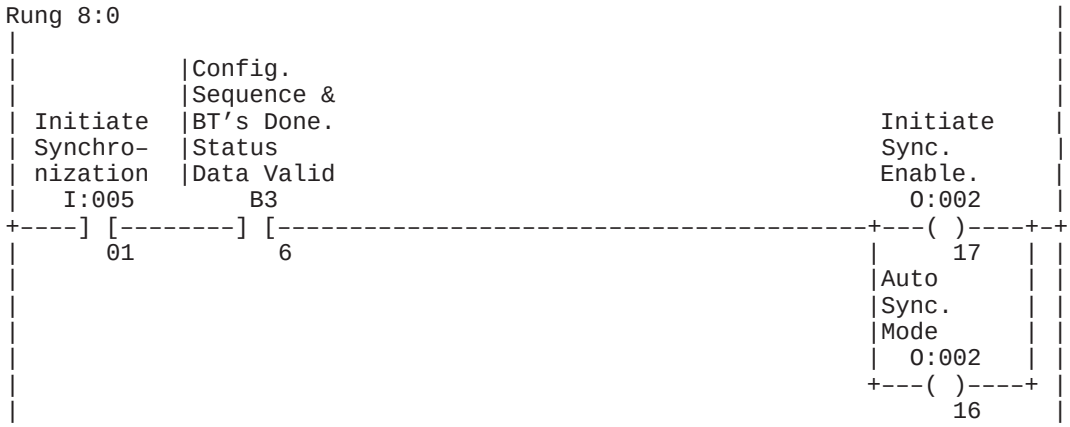
The following pages contain an application ladder program that accomplishes synchronization through the use of the PID control instruction available in Allen-Bradley 6200 software.

Continued on next page.

Synchronization Utilizing the 6200 PID Instruction Continued

Rung 8:0

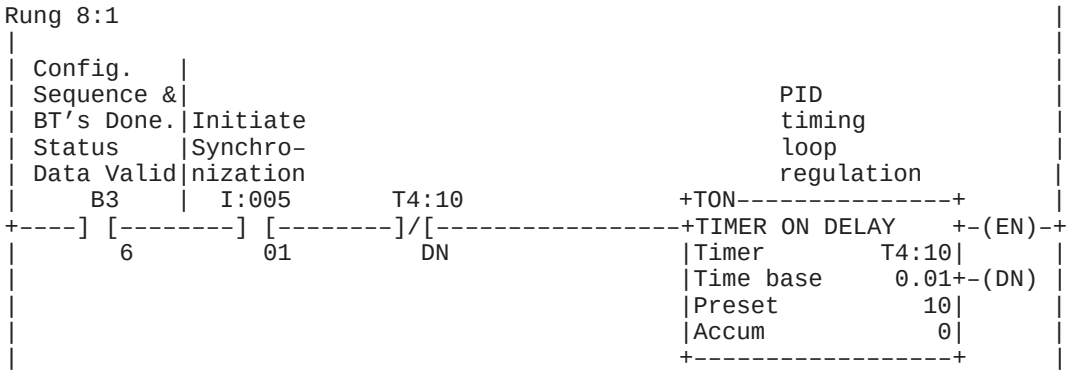
Once the LSM has been successfully configured, (Bit B3/6 set),the synchronization of two voltage busses may begin. Synchronization in this example is enabled manually by a user input switch (Input I:005/01). Once these two inputs are set, synchronization in the Automatic Synchronization mode will be initiated in the LSM (O:002/16 and O:002/17 set).



Rung 8:1

Once the LSM has been successfully configured, and the user has initiated the synchronization process, timer T4:10 will be enabled and will regulate the operation of the PID control instructions used to correct Sync. Bus Frequency and Sync. Bus Phase (the frequency of the Synchronization Bus will be synchronized before phase). Because the LSM update rate for Synchronizing Bus error parameters is 100 ms, the PID instructions will be allowed to operate only when timer T4:10 has accumulated to an equal time of 100 ms. This 100 ms delay between PID updates will allow time for new frequency and phase error parameters to be updated and converted into the appropriate number of counts for the PID algorithm.

Note: The **loop update time** parameter (N75:13 & N79:13 within the two PID instructions) must match the preset time of the regulating timer (T4:10). Since error updates occur every 100 ms, it is necessary that the PID instruction is notified of the update rate so that the integral and derivative calculations within the PID algorithm function accurately. When timer T4:10 completes a 100 ms cycle, the done bit (T4:10/DN) will reset the timer, and once again the cycle that regulates the PID process will be repeated.



Rung 8:2

Rung 8:2 will allow the user to manually select which mode of the **Frequency adjust PID** Instruction to operate in (Manual or Automatic). When Input switch I:005/02 is open, output N75:0/01 will be set, and the Frequency PID Instruction will operate in **manual control** mode. (N75:0/01 is the operation mode select bit within the **PID Control Block** integer file.) When operating in manual mode, the **Tieback** integer file, (N76:0), located within the Frequency PID control instruction, may be loaded with a desired number of analog counts, (0–4095), to be output to an analog output module. When Input I:005/02 is switched to a closed position, output N75:0/01 will be reset, and the PID instruction will operate in **automatic control** mode. When operating in automatic mode, the PID algorithm will take over and produce analog output based on the user defined PID setpoint and the PID gains. Utilizing manual mode operation will allow for easier tuning of the PID instruction gains. In this particular application, the output to an analog output module is held at a constant faulty count as a result of the tieback file being output during PID manual mode operation. When switching back into automatic mode the PID algorithm will correct the output based on the setpoint and the PID gains.

Continued on next page.

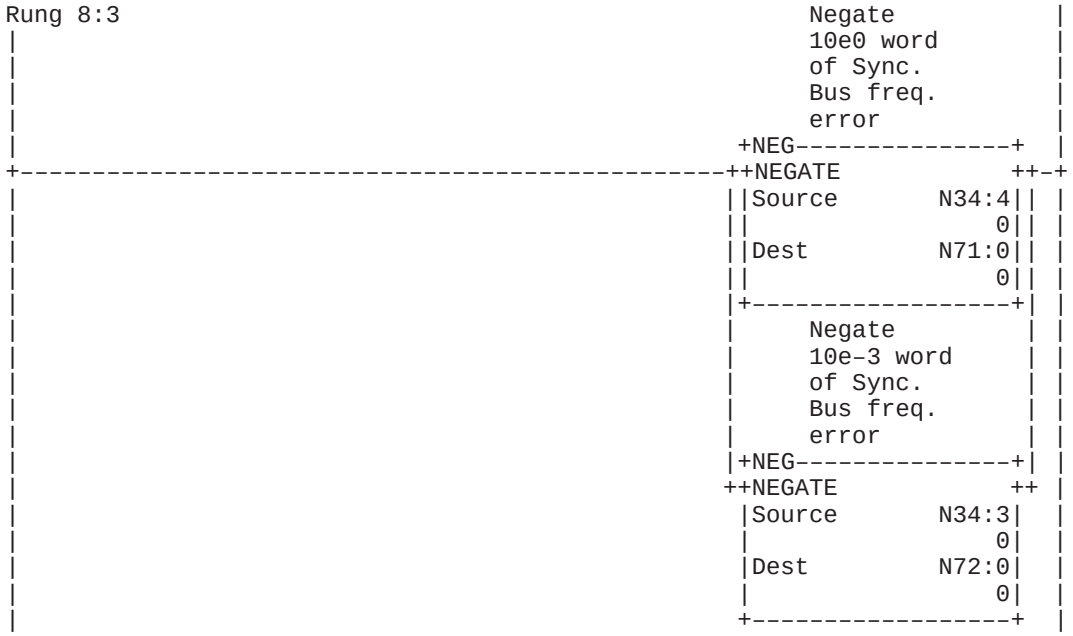
Synchronization Utilizing the 6200 PID Instruction Continued

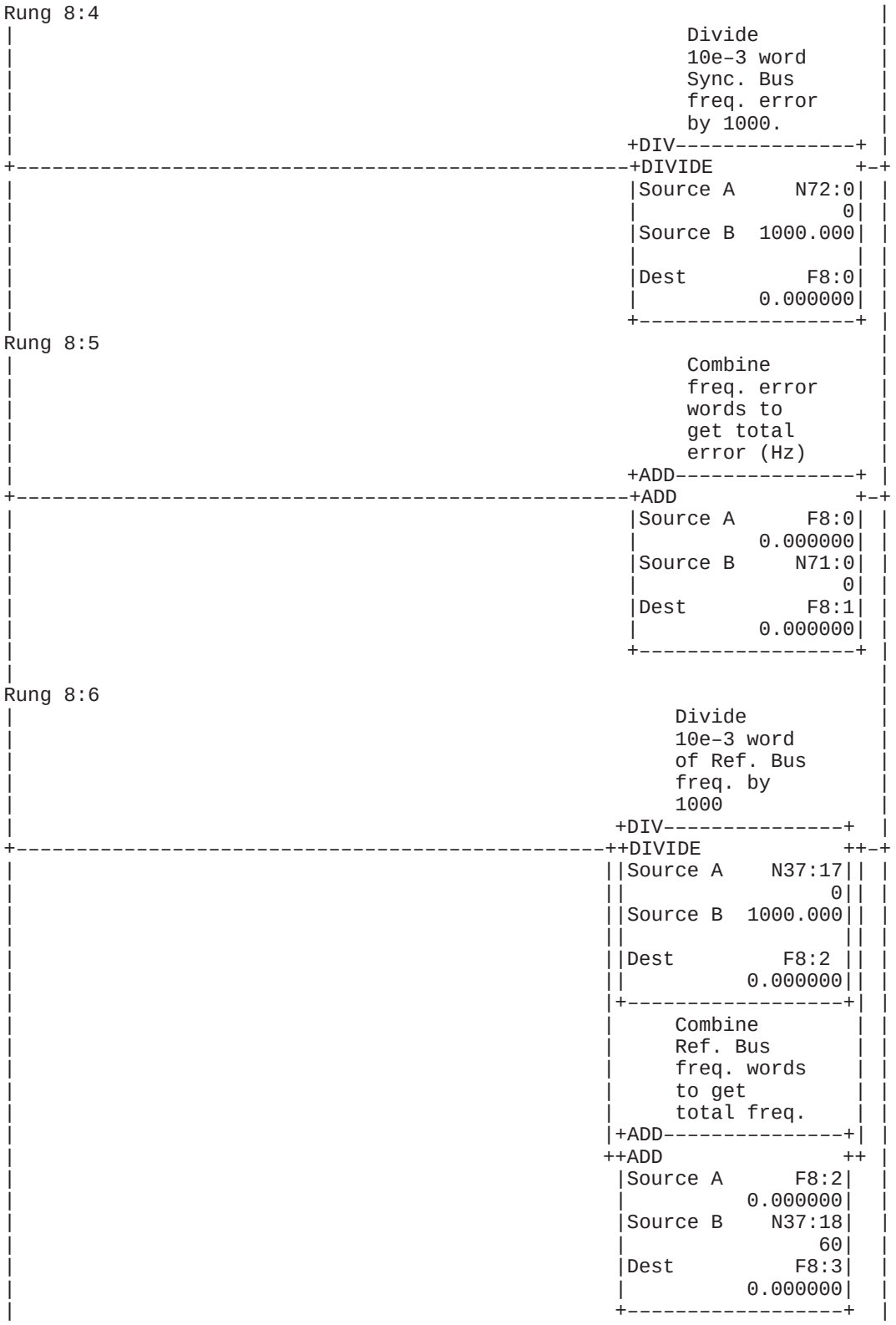
Rungs 8:3–8:8

Rungs 8:3–8:8 convert the Synchronization Bus Frequency Match Error into a representative number of analog counts to be processed by the frequency adjust PID instruction. The conversion factors for Hz, RPM, and analog counts are as follows:

$$\left[\frac{1Hz}{30RPM}\right] \times \left[\frac{1RPM}{2.1505\ counts}\right] = \left[\frac{1Hz}{64.52\ counts}\right]$$

It was necessary to convert the Synchronizing Bus frequency match error in Hertz into analog counts to obtain higher resolution in the PID calculations. Rungs 8:3–8:5 negate each word of the Synchronizing Bus Frequency Match Error and then combine the integer and the decimal portion to obtain the total error in Hertz. Rungs 8:6 and 8:7 calculate the actual Reference Bus frequency and the actual Synchronizing Bus frequency. By negating the total Synchronizing Bus frequency match error, and then adding the negated error to the Reference Bus frequency, the actual Synchronizing Bus frequency is obtained. In this application, the Synchronizing Bus frequency is not obtained directly from the LSM Monitoring Parameters Tables because they are updated at 1 second when synchronization is active. To obtain frequency at a faster rate, it must be obtained as the Synchronizing Bus Frequency Match Error. Rung 8:8 converts the actual Synchronizing Bus frequency into an equivalent number of analog counts to be input into the PID instruction.





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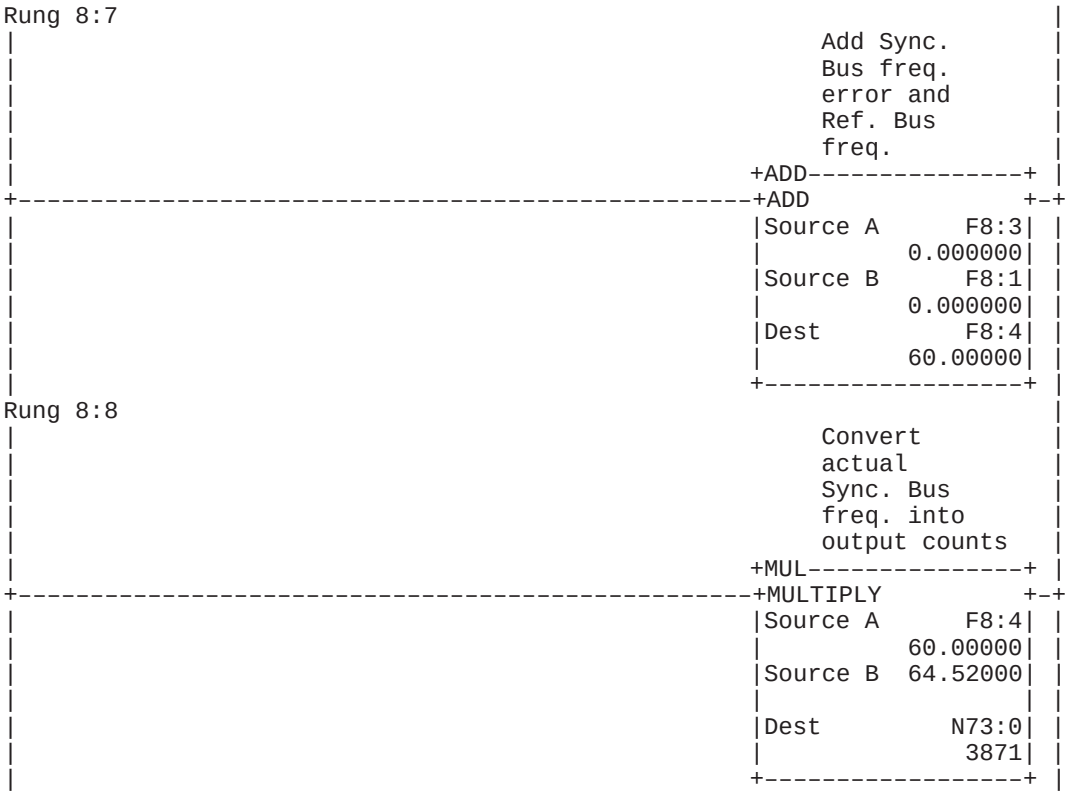
Synchronization Utilizing the 6200 PID Instruction Continued

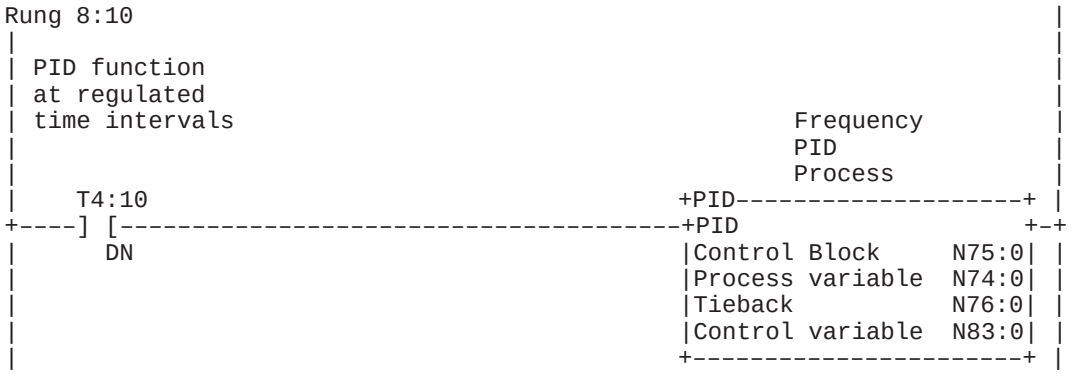


Rung 8:9

When the PID regulating timer completes one 100 ms cycle, the PID process is allowed to begin, at which instant the latest Synchronizing Bus frequency represented in analog output counts is moved into the process variable (N74:0) of the PID control instruction. This is done to ensure that the PID process variable will not change during the operation of the PID algorithm.

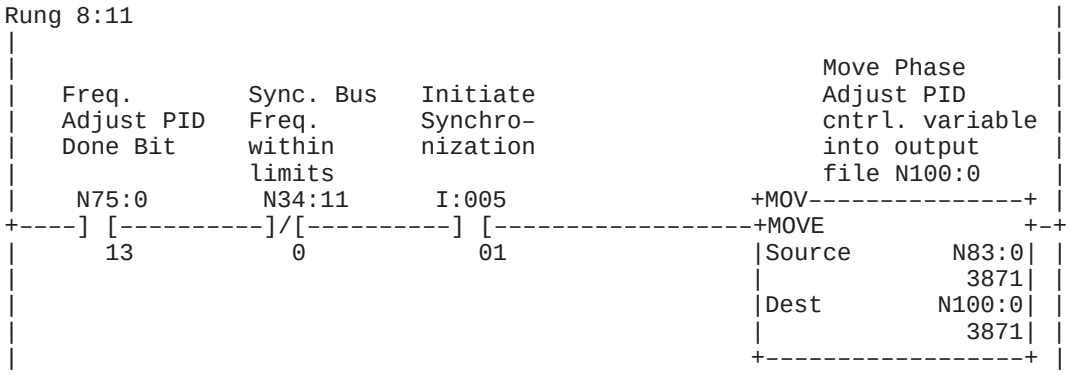
Rung 8:10

The frequency adjust PID control instruction may be appropriately tuned by altering the PID Control Block integer file (N75:0). This **Control Block** file may be accessed through the user interactive data control screen (using 6200 software, highlight the PID instruction and press F8. Included at the end of this application ladder program are the actual data control screens used in this synchronization program). The **Process Variable** (N74:0) is the input to the PID instruction in calculated counts, and the **Control Variable** (N83:0) is the output to the Analog Output Module in counts (0–4095). When operating in manual mode, the **Tieback** integer file, (N76:0), may be preset with a desired number of analog counts, (0–4095), to be output to the Analog Output Module. Because the PID process is application specific, PID parameters may require specific tuning for particular applications. The existing PID parameters in this program are unique to this application. Please refer to Chapter 14 in the *Allen-Bradley PLC-5 Programming Software Instruction Set Reference* for further information on PID set-up and tuning methods.



Rung 8:11

While the Synchronizing Bus Frequency is out of limits, the output calculated in the frequency adjust PID instruction will be moved to the BTW output file N100:0. If the user has initiated the synchronization process (I:005/01 set), new PID output to the block transfer output file N100:0 will be updated each time the frequency adjust PID instruction completes a calculation cycle (N75:0/13 set).



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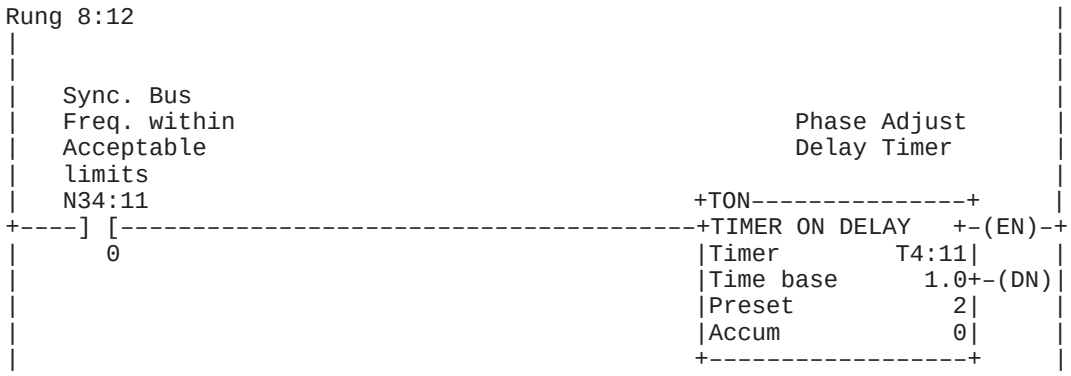
Synchronization Utilizing the 6200 PID Instruction Continued

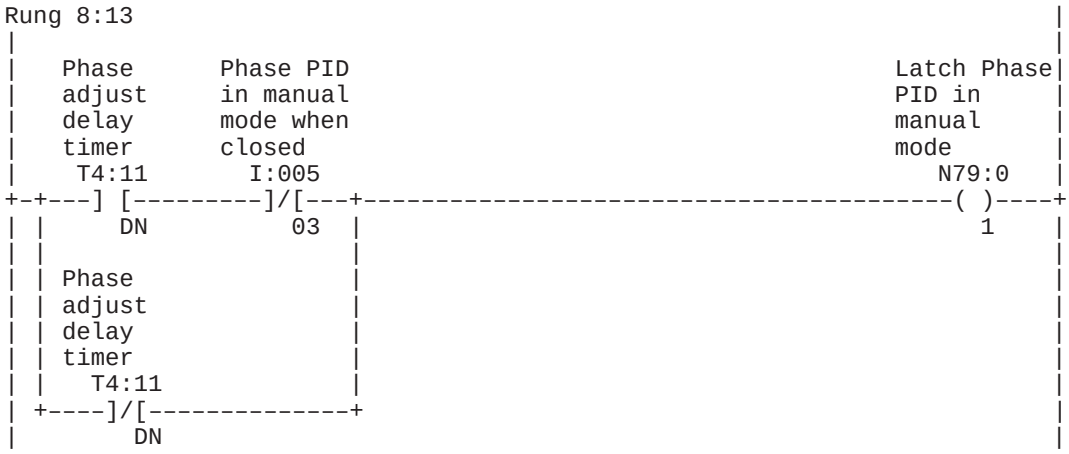
Rung 8:12

Rung 12 will be activated at the moment that the Synchronizing Bus frequency reaches an acceptable value. Timer T4:11 is used to create a delay period when transferring from frequency adjust PID operation to phase adjust PID operation. Before the phase adjust PID instruction is allowed to operate, there must be a short delay to allow the rate of change of phase error to stabilize. Timer T4:11 will allow for a smooth transition between frequency correction and phase correction.



Rung 8:13

Rung 13 allows the user to manually select which mode of the **Phase Adjust PID** instruction to operate in (Manual or Automatic). Input I:005/03 is the operation mode select input for the phase match PID Instruction. Immediately after the Synchronizing Bus frequency enters the acceptable limits, delay timer T4:11 in rung 12 will be enabled. During the delay period, the phase adjust PID instruction will be held in manual mode during which time the output will be held at the number of counts in the **tieback file (N83:0)** within the **phase adjust** PID instruction. The tieback file for the phase adjust PID instruction will be set at the **control variable (N83:0)** of the **frequency adjust** PID instruction. When the phase adjust PID instruction is operating in manual mode, the output from the phase adjust PID instruction will be "tied back" to the actual corrected output from the frequency adjust PID instruction. When timer T4:11 has finished its delay period, the operator will then control which mode the phase adjust PID instruction will operate in. User input I:005/03 will determine which mode of operation is utilized after timer T4:11 delay period.



Rung 8:14

The Synchronization Bus phase match error (N34:5) supplied by the LSM on each 100 ms update cycle will be within the range of (–180° – +180°). The phase adjust PID instruction requires that the process variable input is a positive number. By adding 180° to the actual error, the phase error is scaled to a positive range of 0° to 360°. The setpoint for the phase adjust PID instruction should be set at 180° for 0° actual phase match.

Rung 8:15

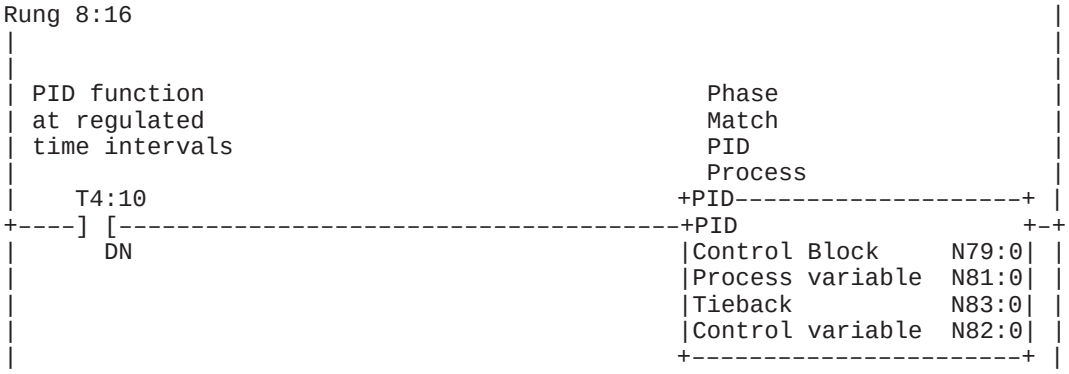
As the PID regulating timer T4:10 completes each 100 ms cycle, the PID process is allowed to begin, at which instant the latest Synchronizing Bus phase match error represented in degrees (0–360) is moved into the process variable (N81:0) of the PID control instruction. This is done to ensure that the PID process variable will not change during the operation of the PID algorithm.

Continued on next page.

Synchronization Utilizing the 6200 PID Instruction Continued

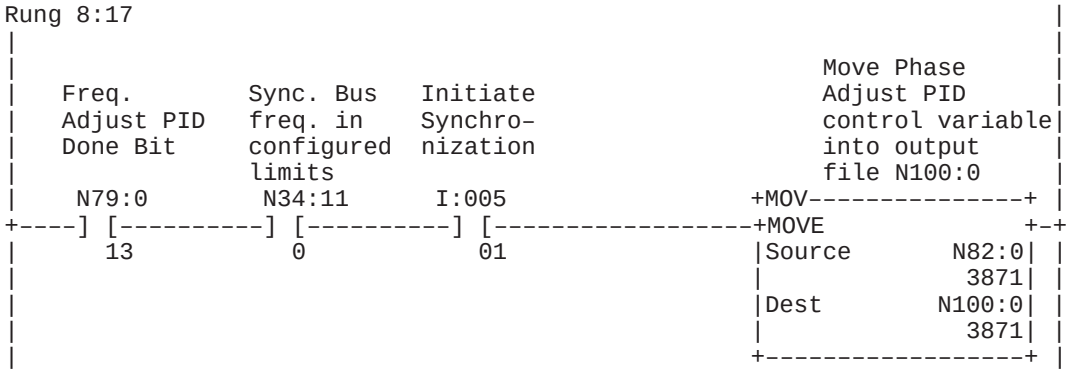
Rung 8:16

The phase match PID **Control Block** file (N79:0) may be accessed through the user interactive data monitor screen (highlight the PID instruction and press F8). The **Process Variable** (N81:0) is the input to the PID in degrees (0–360), and the **Control Variable** (N82:0) is the output to the Analog Output Module in counts (0–4095). The phase adjust PID instruction will not be allowed to operate until each 100 ms cycle of T4:10 is done, and until the Synchronizing Bus frequency is within factory configuration limits. Because the phase match PID will not operate until the Synchronizing Bus frequency is within error limits, the **tieback** of the phase match PID has been set to the control variable (N83:0) of the frequency adjust PID control. Refer to rung description **8:2** located earlier in the document for further information regarding manual and automatic PID control (refer also to rung **8:13** for further information regarding transferring between frequency and phase PID correction.)



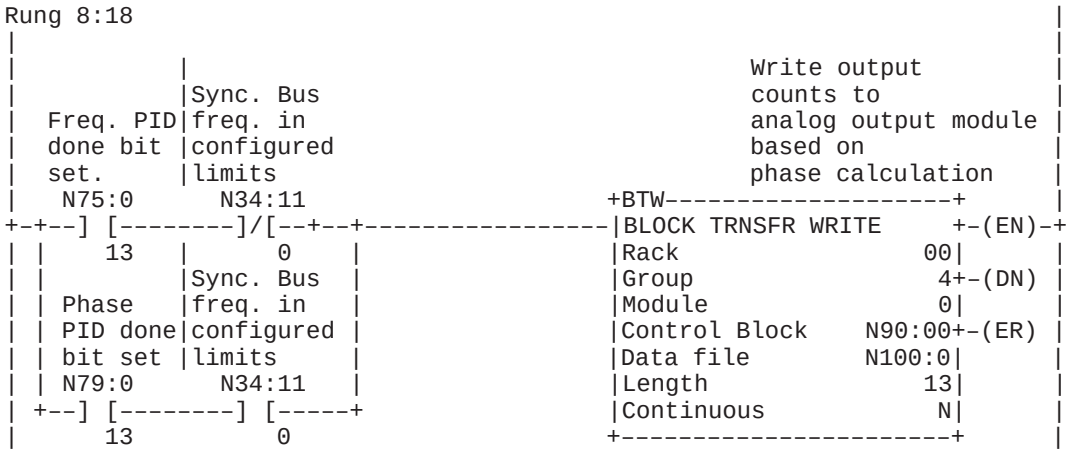
Rung 8:17

While the Synchronizing Bus Frequency is within the configured limits, the output calculated in the phase adjust PID instruction will be moved to the BTW output file N100:0. If the user has initiated the synchronization process (I:005/01 set), new output to the block transfer output file will be updated each time the phase adjust PID instruction completes a calculation cycle. Phase adjust PID done bit N79:0/13 will be set each time the PID instruction completes a calculation cycle. At times when data generated by the frequency adjust PID instruction is being moved into output file N100:0, rung 8:17 will not be active. Either frequency PID data or phase PID data will be moved into output file N100:0. Data transfer from both PID instructions to output file N100:0 will never occur simultaneously.



Rung 8:18

While the Synchronizing Bus frequency is out of configured limits, the frequency adjust PID instruction will be the sole controller of BTW output. After each frequency adjust PID calculation cycle, an updated number of counts will be output to an analog output module. After frequency enters the acceptable limits, the phase adjust PID instruction will be the sole controller of BTW output. Each time the phase adjust PID instruction completes a calculation cycle, the new number of counts generated by the phase adjust PID instruction will be updated.



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Synchronization Utilizing the 6200 PID Instruction Continued

Rung 8:19

If voltage control has been enabled (I:005/04) set, the motorized potentiometer used to raise and lower the Synchronizing Bus voltage is enabled (O:001/02 set).

```
Rung 8:19                                                                  |
|                                                                          |
|  Voltage                                                    Enable       |
|  control                                                    pot. to      |
|  enable                                                     raise/       |
|                                                             lower Sync   |
|                                                             Bus voltage  |
|   I:005                                                       O:001      |
+----] [-------------------------------------------------------( )-------+
|       4                                                        02        |
```

Rung 8:20

If the “Raise Voltage” discrete input (I:002/16) from the LSM is set, the potentiometer is appropriately adjusted through output O:001/01.

```
Rung 8:20
| Raise                                                                    |
| Voltage                                                     Raise        |
| LSM                                                         Voltage      |
| Output                                                      Output       |
|   I:002                                                       O:001      |
+----] [-------------------------------------------------------( )-------+
|      16                                                        01        |
```

Rung 8:21

If the “Lower Voltage” discrete input (I:002/15) from the LSM is set, the potentiometer is appropriately adjusted through output O:001/00.

```
Rung 8:21
| Lower                                                                    |
| Voltage                                                     Lower        |
| LSM                                                         Voltage      |
| Output                                                      Output       |
|   I:002                                                       O:001      |
+----] [-------------------------------------------------------( )-------+
|      15                                                        00        |
```

Rung 8:22

When Synchronizing Bus frequency, phase, and voltage are all within the configured limits for the specified delay window, the breaker is closed between the Synchronization Bus and the Reference Bus.

```
Rung 8:22                                                                    |
|                                                                            |
| Close                                                            Close     |
| breaker                                                          breaker   |
| input                                                            output    |
| from                                                             from      |
| LSM                                                              PLC       |
|   I:002                                                            O:001   |
+----] [-------------------------------------------------------------( )--+
|      03                                                              17    |
|                                                                            |
|                                                                            |
|-----------------------------[END OF FILE]------------------------------|
```

Note: Rung 8:10 refers to the PID control block screen shown below. Please see the *Allen-Bradley PLC-5 Programming Software Instruction Set Reference* manual for directions on how to change PID control block parameters.

```
equation: 0 (0:AB/1:ISA)             feed forward:       0
                  mode: 1 (0:auto/1:manual)    max scaled input:    4095
                 error: 0 (0:SP-PV/1:PV-SP)    min scaled input:       0
       output Limiting: 0 (0:NO/1:YES)                deadband:       0
       set output mode: 0 (0:NO/1:YES)       set output value %:       0
     setpoint scaling: 0 (0:YES/1:NO)         upper CV limit %:     100
     derivative input: 1 (0:PV/1:error)       lower CV limit %:       0
    last state resume: 0 (0:NO/1:YES)          scaled PV value:    3869
      deadband status: 0                          scaled error:       2
  upper CV Limit alarm: 0                         current CV %:      94
  lower CV Limit alarm: 0
 setpoint out of range: 0
              PID done: 0                      (scaled) setpoint:    3871
          PID enabled: 0          proportional gain (Kp) [.01]:      15
                                 integral gain (Ki) [.001/secs]:     900
                                derivative gain (Kd) [.01 secs]:       2
                                    loop update time [.01 secs]:       5
Enter value or press <ESCAPE> to exit monitor.
N75:0/0 = _
Rem RUN    Forces:None      Data:Formatted              5/40 Addr 0
```

Synchronization through LSM Discrete I/O

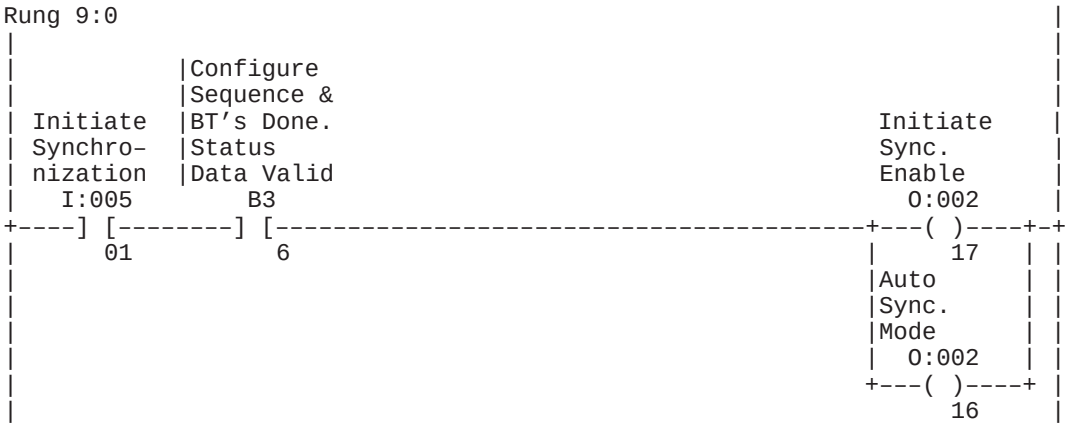
Another feasible alternative to achieving synchronization between an alternator (Synchronizing Bus) and Reference Bus would be through the use of discrete error signals supplied by the LSM. When synchronization in the LSM is active in “Auto Synchronization” mode, the LSM has the ability to issue the appropriate error signals based on the condition of the voltage, frequency and phase. When the Synchronizing Bus parameters of voltage, frequency or phase fall out of the specified LSM Factory Configuration Limits set by the user, the LSM will issue any pertinent error signals. When each of the necessary synchronization parameters for the Synchronizing Bus are acceptable, the LSM will issue a “Close Breaker” discrete output to the PLC. With these discrete outputs from the LSM occurring immediately, the PLC can make the proper corrections on each of the parameters until the two busses are synchronized and the LSM discrete outputs are no longer issued.

Continued on next page.

Synchronization through LSM Discrete I/O Continued

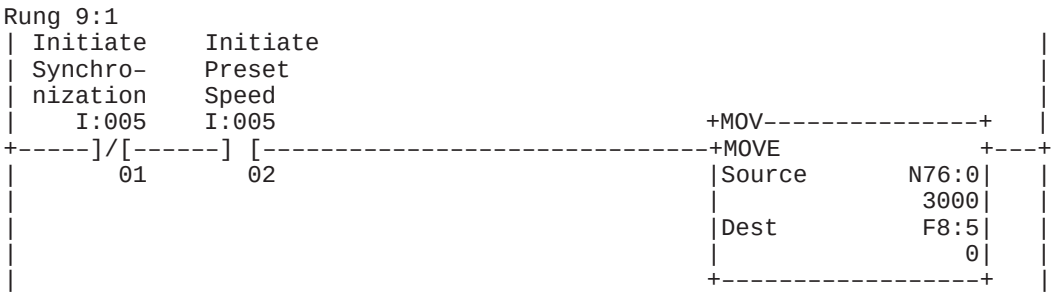
Rung 9:0

Once the LSM has been successfully configured, (Bit B3/6 set), synchronization process may be allowed to start. Synchronization is enabled manually by a switch on a discrete input module (Input I:005/01). Once these two inputs are set, synchronization in the Automatic Synchronization mode will be initiated in the LSM.



Rung 9:1

The operation of the synchronization process in the LSM requires that a synchronizing bus voltage is present. Synchronization may be initiated (user supplied input I:005/01 set), but it will not function if there is no voltage on the Synchronizing Bus. In rung 9:1, an initial preset speed for the alternator may be established while synchronization is not initiated. By switching input I:005/02 to a closed position before synchronization is initiated, the generator will be held at the desired speed placed in file N76:0 until synchronization is initiated and begins to operate (the preset speed placed in file N76:0 should be represented in analog counts, 0–4095).



Rung 9:2

Timer T4:12 is used to regulate the update rate of the analog output (N100:0) *based on Synchronizing Bus frequency error corrections.* With each timer completion of 100 ms (which is also the LSM update rate for "Synchronizing Bus Error Parameters"), a preset, constant number is either added to or subtracted from the number of analog counts calculated during the previous program scan. The timer regulates how often the BTW output file is updated.

```
Rung 9:2
|  T4:12                                        +TON---------------+      |
+--]/[-----------------------------------------+TIMER ON DELAY    +-(EN)-+
|    DN                                         |Timer        T4:12|      |
|                                               |Time base     0.01+-(DN) |
|                                               |Preset          10|      |
|                                               |Accum            0|      |
|                                               +------------------+      |
```

Rung 9:3

Timer T4:13 is used to regulate the update rate of the analog output (N100:0) *based on Synchronizing Bus phase error corrections.* This timer and the phase correction update values will be active only when I:002/13 and I:002/14 are true (Both inputs are LSM discrete inputs representing Frequency Adjust–Lower Speed/Raise Speed). When each of these inputs are low, the Synchronizing Bus frequency errors are within the LSM Factory Configuration Parameters for Frequency Match Error Acceptance limits. With each timer completion of 350 ms, a preset, constant number is either added to or subtracted from the number of analog counts calculated during the previous program scan. The longer timing period of T4:13 used during phase correction is necessary to maintain a slightly overdamped output response. The timer regulates how often the BTW output file is updated.

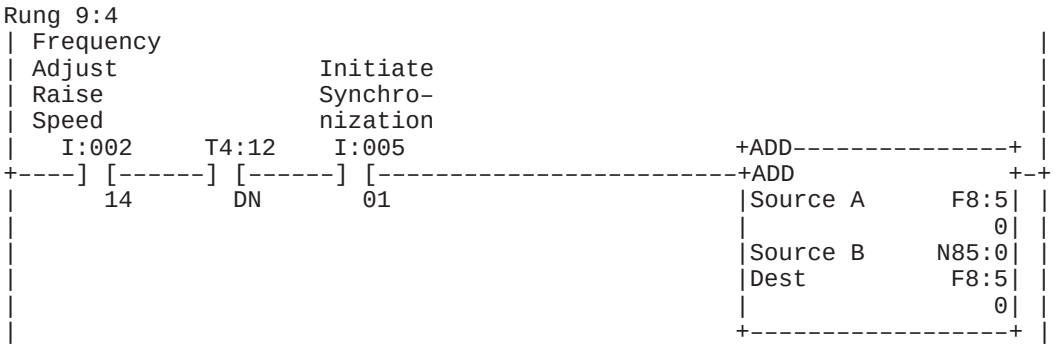
```
Rung 9:3
|  T4:13   I:002   I:002                      +TON---------------+      |
+--]/[-----]/[-----]/[----------------------+TIMER ON DELAY    +-(EN)-+
|    DN      13      14                      |Timer        T4:13|      |
|                                            |Time base     0.01+-(DN) |
|                                            |Preset          35|      |
|                                            |Accum            0|      |
|                                            +------------------+      |
```

Rung 9:4

Input I:002/14 is the "Raise Speed-Frequency Adjust" discrete input to the processor from the LSM. When this input is set, the number of output counts to the analog output module must be increased, which subsequently will raise the speed of the generator. The total number of output counts will be increased by the value in file N85:0. In the event that the generator speed is too low, the LSM input to the processor (I:002/14) will be set, but the number of analog output counts in file N100:0 will be adjusted only when timer T4:12 completes a 100 ms cycle (T4:12/DN set), and when synchronization has been initiated in the LSM (I:005/01 set).

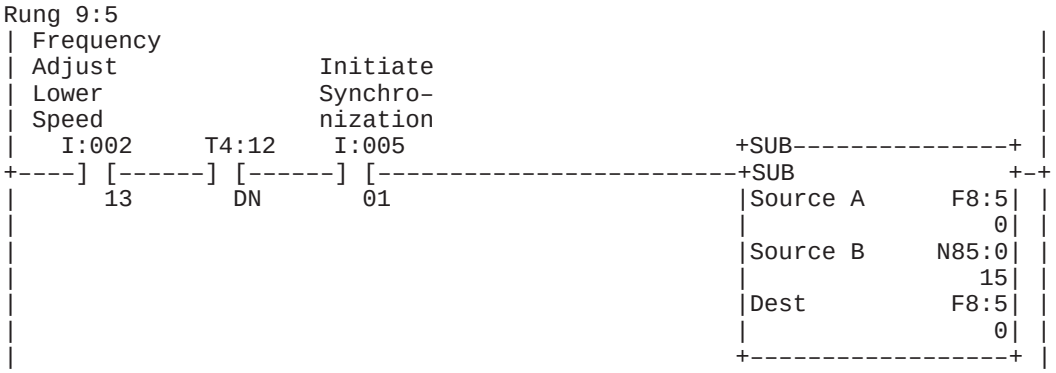
Continued on next page.

Synchronization through LSM Discrete I/O Continued



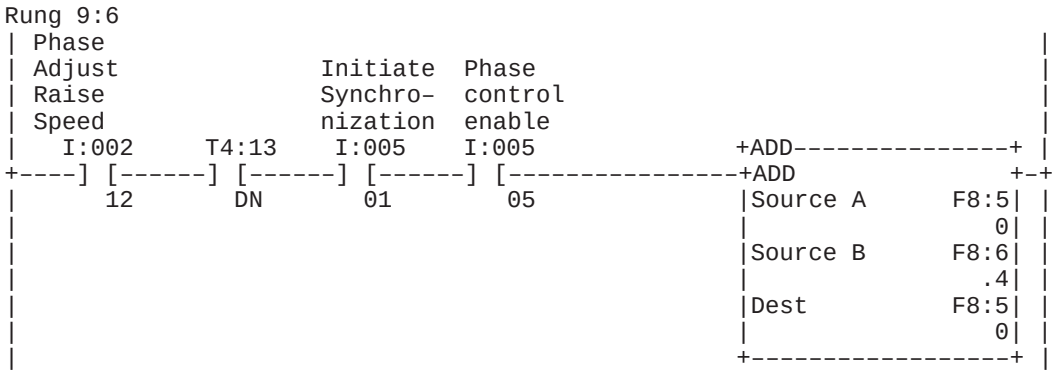
Rung 9:5

Input I:002/13 is the “Lower Speed-Frequency Adjust” discrete input to the processor from the LSM. When this input is set, the number of output counts to the analog input module must be decreased, which subsequently will lower the speed of the generator. The total number of output counts will be decreased by the value in file N85:0. In the event that the generator speed is too high, the LSM input to the processor (I:002/13) will be set, but the number of analog output counts in file N100:0 will be adjusted only when timer T4:12 completes a 100 ms cycle (T4:12/DN set), and when synchronization has been initiated in the LSM (I:005/01 set). Note that in the two rungs used for frequency adjust (9:4 and 9:5), the constant used for the addition and subtraction is greater than the “phase adjust” constant used in rungs 9:6 and 9:7. When speaking of generator speed control in terms of frequency and phase, the frequency regulation should be considered as the coarse adjust for generator speed, while phase regulation should be considered as the fine adjust for generator speed.



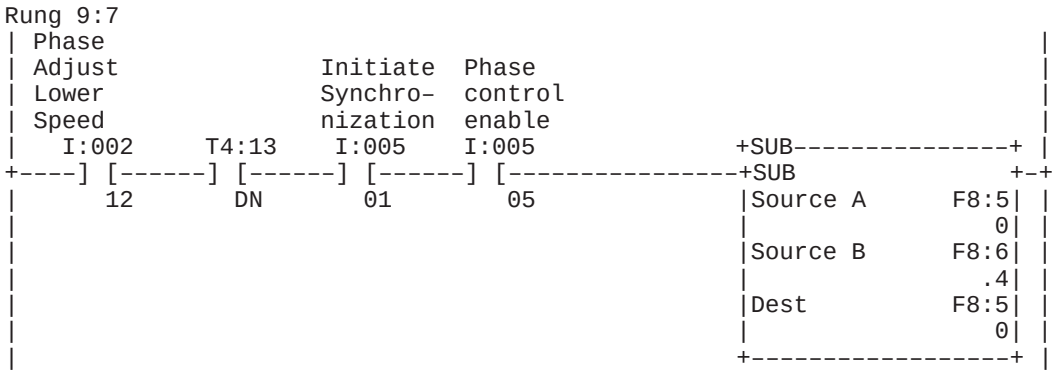
Rung 9:6

Input I:002/12 is the “Raise Speed-Phase Adjust” discrete input to the processor from the LSM. When this input is set, the number of output counts to the analog input module must be increased, which subsequently will raise the speed of the generator. The total number of output counts will be increased by the decimal in file F8:6. In the event that the generator speed is not high enough, the LSM input to the processor (I:002/12) will be set, but the number of analog output counts in file N100:0 will be adjusted only if synchronization has been initiated in the LSM (I:005/01 set), the Phase control has been enabled (I:005/05 set), and timer T4:13 has completed a 350 ms cycle (T4:13/DN set. Assuming frequency is within acceptable limits).



Rung 9:7

Input I:002/11 is the “Lower Speed-Phase Adjust” discrete input to the processor from the LSM. When this input is set, the number of output counts to the analog input module must be decreased, which subsequently will lower the speed of the generator. The total number of output counts will be decreased by the decimal in file F8:6. In the event that the generator speed is not high enough, the LSM input to the processor (I:002/12) will be set, but the number of analog output counts in file N100:0 will be adjusted only if synchronization has been initiated in the LSM (I:005/01 set), the Phase control has been enabled (I:005/05 set), and timer T4:13 has completed a 350 ms cycle (T4:13/DN set. Assuming frequency is within acceptable limits).

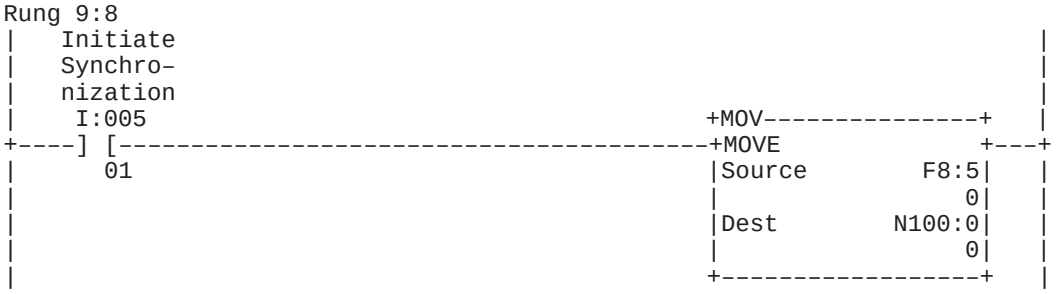


Continued on next page.

Synchronization through LSM Discrete I/O Continued

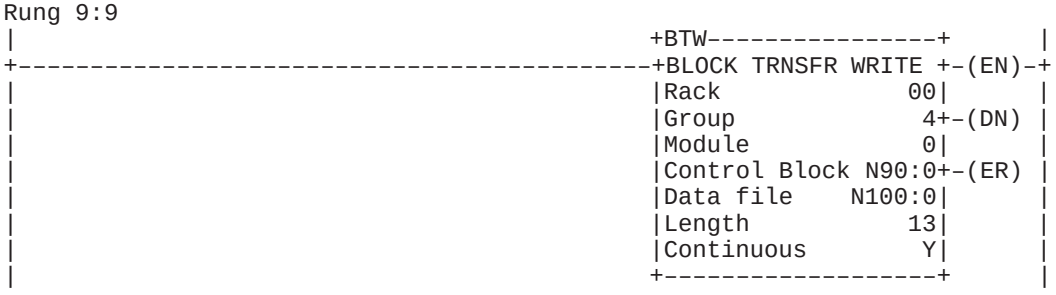
Rung 9:8

If the synchronization process has been initiated (I:005/01 set), the latest number of counts in file F8:5 will be moved into BTW output file N100:0.



Rung 9:9

Rung 9:9 contains the Block Transfer Write that will output the analog counts in file N100:0 to the analog output module. This BTW rung will be true upon each program scan, and will continuously output the current value located in file N100:0. The BTW will continually send the updated number of counts located in file N100:0.



Rung 9:10

Once the frequency error and the phase displacement error have both been compensated for, the Synchronizing Bus voltage is the remaining parameter that must be synchronized. If voltage control has been enabled (I:005/04) set, the motorized potentiometer used to raise and lower the Synchronizing Bus voltage is enabled (O:001/02 set).

Rung 9:11

If the “Raise Voltage” discrete input (I:002/16) from the LSM is set, the potentiometer is appropriately adjusted through output O:001/01.

```
Rung 9:11
| Raise                                                                 |
| Voltage                                                    Raise      |
| LSM                                                        Voltage    |
| Output                                                     Output     |
|   I:002                                                      O:001    |
+----] [-----------------------------------------------------------( )-----+
|      16                                                        01     |
```

Rung 9:12

If the “Lower Voltage” discrete input (I:002/15) from the LSM is set, the potentiometer is appropriately adjusted through output O:001/00.

```
Rung 9:12
| Lower                                                                 |
| Voltage                                                    Lower      |
| LSM                                                        Voltage    |
| Output                                                     Output     |
|   I:002                                                      O:001    |
+----] [-----------------------------------------------------------( )-----+
|      15                                                        00     |
```

Rung 9:13

When Synchronizing Bus frequency, phase, and voltage are all within the configured limits, the breaker between the Synchronization Bus and the Reference Bus is closed.

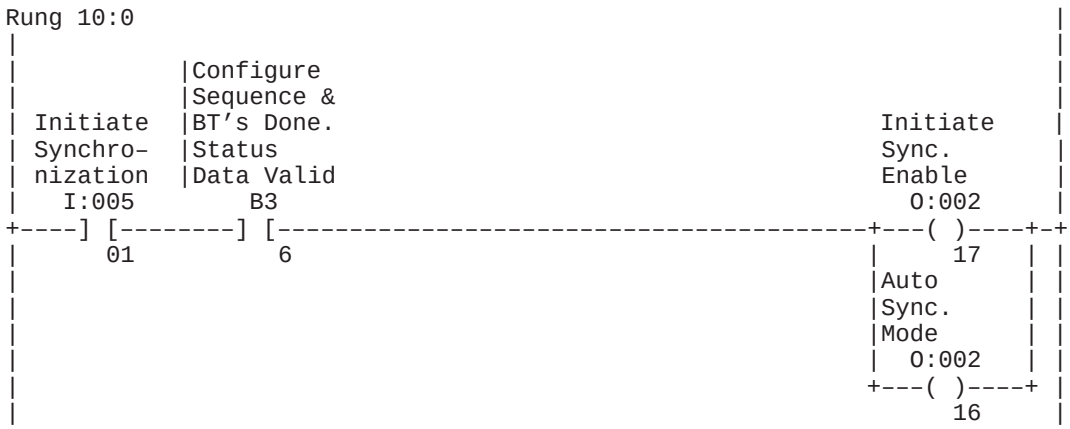
```
Rung 9:13
| Close                                                  Close          |
| breaker                                                breaker        |
| input                                                  output         |
| from                                                   from           |
| LSM                                                    PLC            |
| I:002                                                         O:001    |
+--] [-------------------------------------------------------------( )--+
|    03                                                           17    |
|                                                                       |
+-------------------------[END OF FILE]---------------------------------+
|                                                                       |
```

Synchronization through the Clipped Gain Method

A third method of completing synchronization between an alternator (Synchronizing Bus) and Reference Bus would be through the use of Block Transfer Read (BTR) data tables supplied by the LSM. When synchronization in the LSM is active in “Auto Synchronization” mode, the LSM will provide all data pertaining to each of the voltage busses (refer to Appendix B of the LSM Installation and Operation Manual). When the Synchronizing Bus parameters of voltage, frequency or phase fall out of the specified LSM Factory Configuration Limits set by the user, the error for each parameter provided in the LSM BTR data tables may be manipulated by the user, through a PLC, thus forcing the particular parameter back to an acceptable limit. When each of the necessary synchronization parameters for the Synchronizing Bus are acceptable, the LSM will issue a “Close Breaker” discrete output to the PLC. With the Synchronizing Bus error parameters being updated every 100 ms, the PLC can quickly make the proper corrections on each of the parameters until the two busses are synchronized and the LSM error parameters are acceptable.

Rung 10:0

Once the LSM has been successfully configured, (Bit B3/6 set), the synchronization process may be allowed to start. Synchronization in the LSM, in this application, is enabled manually by a switch on a discrete input module (Input I:005/01). Once these two inputs are set, synchronization in the Automatic Synchronization mode will be initiated in the LSM.



Rung 10:1

Integer files N37:17 and N37:18 contain block transfer data from the LSM representing Reference Bus Frequency. When combined, these two words will equal the total Reference Bus Frequency. The value 64.52 is the factor used to convert Hz to digital counts. The conversion factor used in these application programs is unique to this particular method of alternator speed control. The value stored in file F8:21 will be the value of the Reference Bus Frequency represented in counts (0–4095).

```
Rung 10:1
   freq corr = ((0.001 * reference bus frequency fractional) +
                reference bus frequency whole) * 64.52
|                                        +CPT-------------------------+ |
+----------------------------------------COMPUTE                       +-+
|                                        |Destination           F8:21| |
|                                        |                   3873.781| |
|                                        |Expression                 | |
|                                        |((0.0010000 * N37:17) +    | |
|                                        |N37:18) * 64.52000         | |
|                                        +---------------------------+ |
```

Rung 10:2

Rung 10:2 transfers the setpoint speed used for frequency match to the control variable being used for phase match. In synchronization, the frequency correction is referred to as the coarse adjust. The value in file F8:26 will be further fine tuned for synchronization by adjusting the phase.

```
Rung 10:2
| Close                                                               |
| Breaker                                                             |
| LSM                                                                 |
| Output                                                              |
| CLOSEBREAK                                                          |
|   I:002                                  +MOV--------------------+ |
+----]/[-----------------------------------+MOVE                    +-+
|      03                                  |Source           F8:21| |
|                                          |                3873.781| |
|                                          |Destination      F8:26| |
|                                          |                3873.781| |
|                                          +-----------------------+ |
```

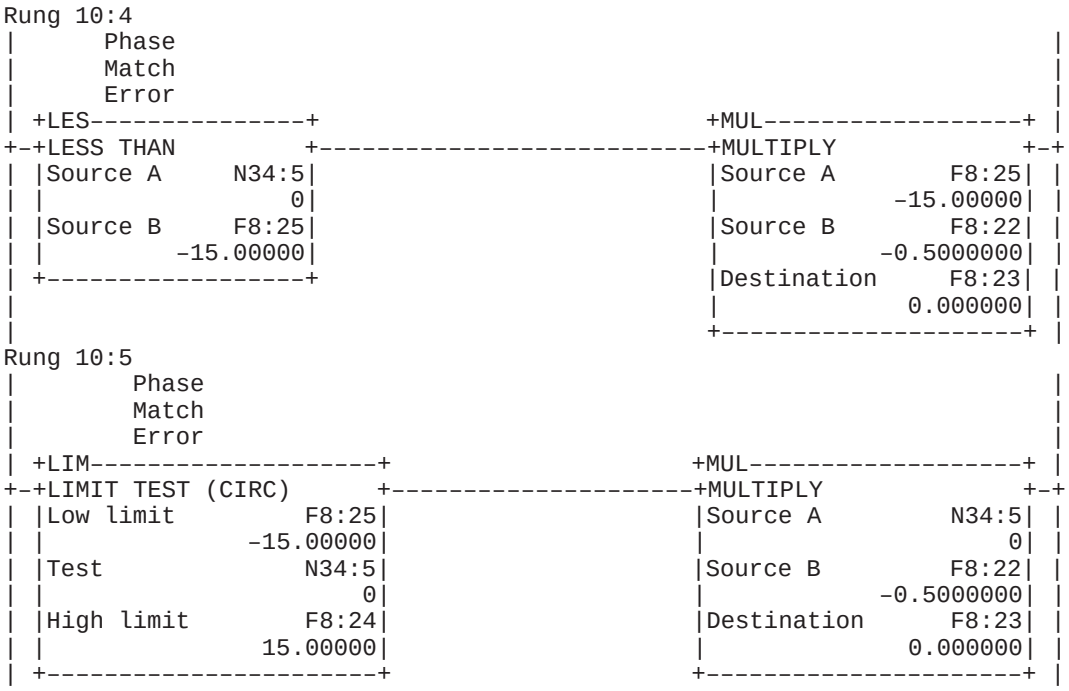
Rungs 10:3–10:5

Rungs 10:3–10:5 correct for phase error by testing to see if it is within a user defined error "window." The files F8:25 and F8:24 represent the error limits used in the Clipped Gain method of error compensation. If the phase error (N34:5) is less than the lower limit or greater than the upper limit, phase correction (F8:23) is calculated by multiplying the phase gain (F8:22) by the lower or upper limit, respectively. If the phase error is within the error window, the phase correction is calculated by multiplying the phase gain by the actual phase error.

```
Rung 10:3
|      Phase                                                          |
|      Match                                                          |
|      Error                                                          |
| +GRT---------------+                     +MUL--------------------+ |
+-+GREATER THAN      +-----------------------+MULTIPLY               +-+
| |Source A     N34:5|                     |Source A          F8:24| |
| |                  0|                     |                15.00000| |
| |Source B     F8:24|                     |Source B          F8:22| |
| |           15.00000|                     |              -0.5000000| |
| +-------------------+                     |Destination       F8:23| |
|                                           |                 0.000000| |
|                                           +-----------------------+ |
```

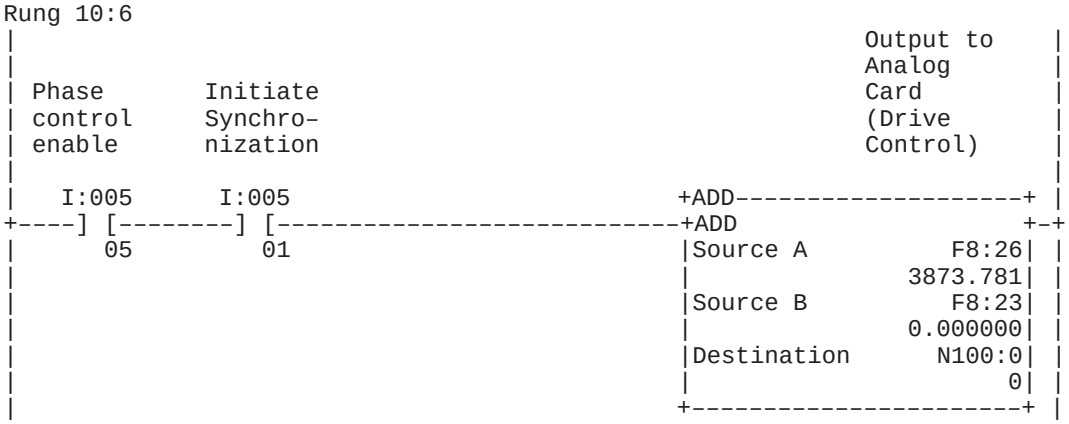

Continued on next page.

Synchronization through the Clipped Gain Method Continued



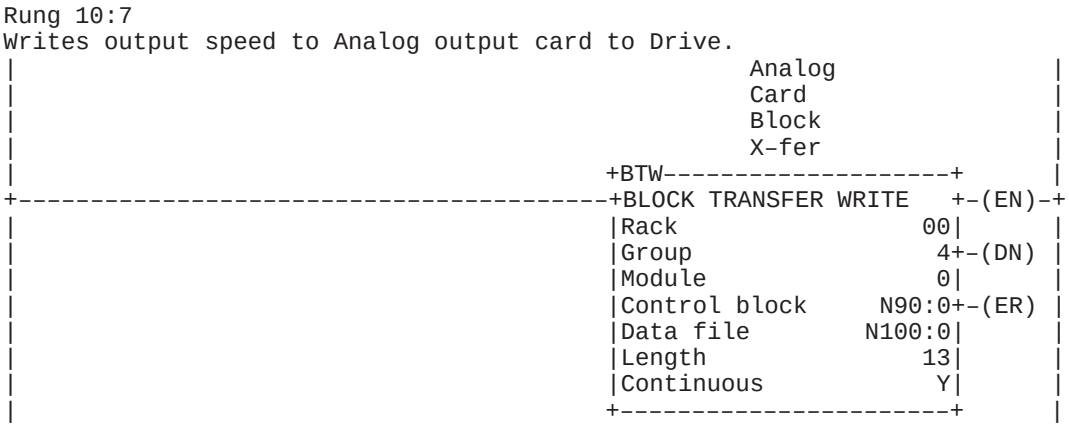
Rung 10:6

If the synchronization process and phase control have been enabled (I:005/05 and I:005/01 set), the phase adjustments are added to the frequency setpoint and stored in BTW output file N100:0.



Rung 10:7

The block transfer write will send the output counts located in file N100:0 to an analog output module located in group 4 of the same rack. The BTW is continuous, and will write the value located in N100:0 upon every program scan.

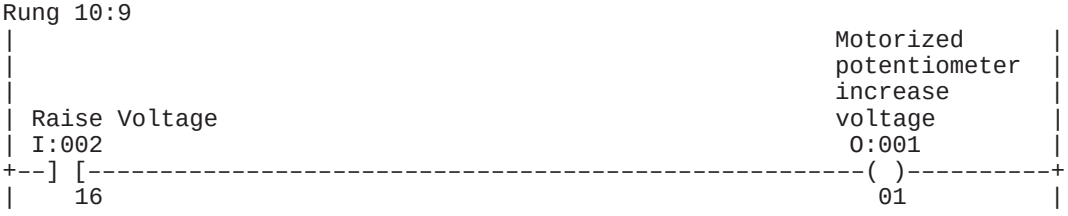


Rung 10:8

Once the frequency error and the phase displacement error have both been compensated for, the Synchronizing Bus voltage is the remaining parameter that must be synchronized. If voltage control has been enabled (I:005/04) set, the motorized potentiometer used to raise and lower the Synchronizing Bus voltage is enabled (O:001/02 set).

Rung 10:9

If the “Raise Voltage” discrete input (I:002/16) from the LSM is set, the potentiometer is appropriately adjusted through output O:001/01.



Rung 10:10

If the “Lower Voltage” discrete input (I:002/15) from the LSM is set, the potentiometer is appropriately adjusted through output O:001/00.

Continued on next page.

Synchronization through the Clipped Gain Method Continued

```
Rung 10:10
|                                                          Motorized      |
|                                                          potentiometer  |
|                                                          decrease       |
| Lower Voltage                                            voltage        |
| I:002                                                     O:001         |
+--] [-----------------------------------------------------( )----------+
|    15                                                       00          |
```

Rung 10:11

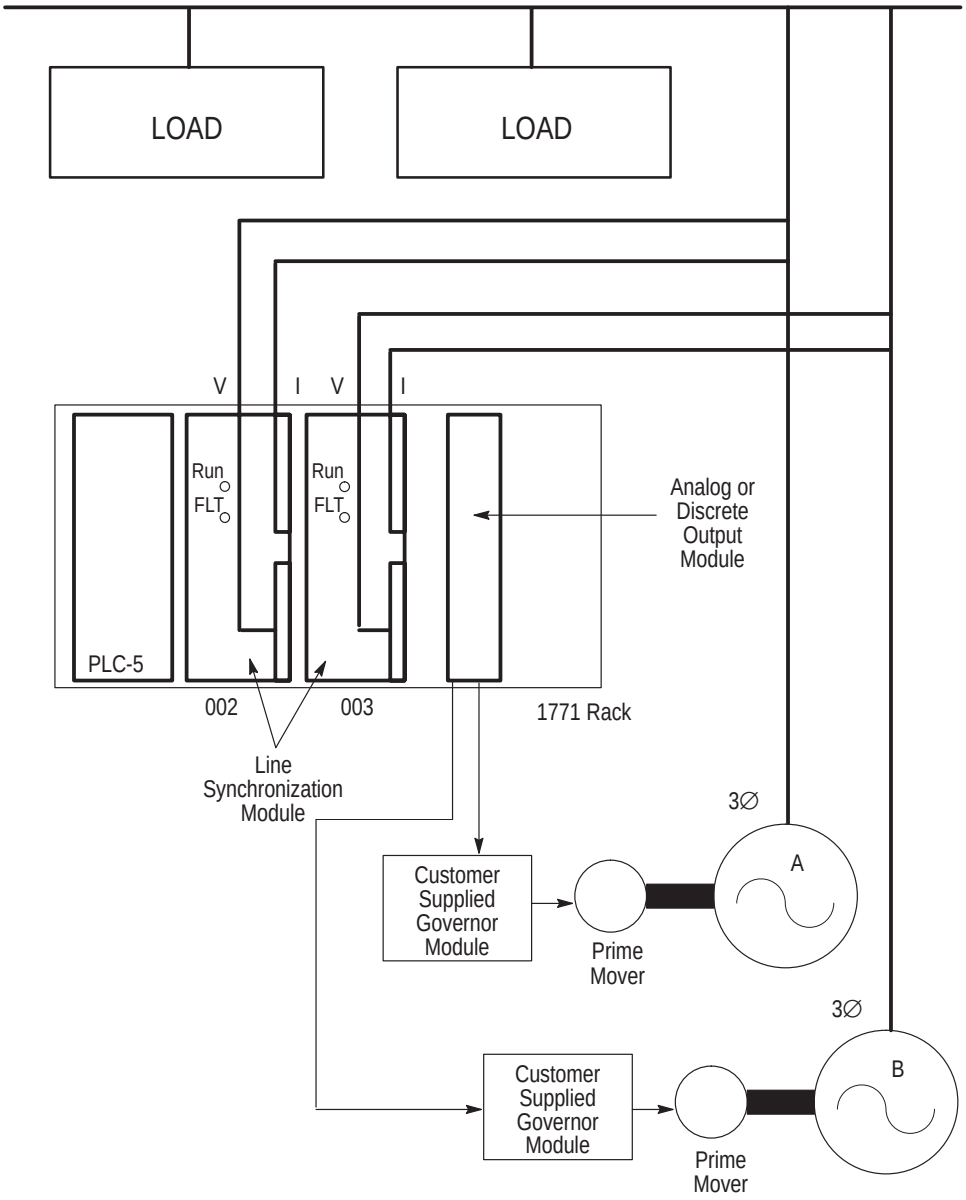
When Synchronizing Bus frequency, phase, and voltage are all within the configured limits, the breaker between the synchronization bus and the reference bus is closed.

```
Rung 10:11
| Close                                                    Close          |
| breaker                                                  breaker        |
| input                                                    output         |
| from                                                     from           |
| LSM                                                      PLC            |
| I:002                                                           O:001   |
+--] [-------------------------------------------------------------( )--+
|    03                                                             17   |
|                                                                        |
+-------------------------[END OF FILE]---------------------------------+
```

Load Sharing Utilizing LSM BTR Data

It is probable that a specific installation will have multiple alternators. These alternators may differ in size or power capacity. In either instance, it may be desirable to balance the sharing of load power between the multiple alternators. This load sharing can be accomplished using the LSM in several ways. The most simple and effective method of load sharing is using one LSM for each alternator to measure the power output of that alternator. Using this power and the maximum, nameplate rated power of the alternator, a percent full-load power can be calculated. Since this number is a percentage, it can be freely compared and/or balanced with other alternators that may not be of the same power capacity. The principle behind load sharing is that all alternators providing power are providing the same percentage of their full-load power. With this balancing method, the operation of alternators of varying sizes is maximized.

November**Figure 4**
Power Bus ∅



Continued on next page.

Load Sharing Utilizing LSM BTR Data Continued

Rung 2:0

The “Maximum Alternator Output Power” located in files N30:22 and N30:23 is a Line Synchronization Module Factory Configuration Parameter. The calculated value in file F8:0 is **Alternator A** Maximum Output Power in units of Megawatts.

```
Rung 2:0
|                                          +CPT--------------------+      |
+------------------------------------------+COMPUTE                +      |
|                                          |Destination        F8:0|      |
|                                          |               637.5000|      |
|                                          |Expression             |      |
|                                          |((N30:23 * 1000.000) + |      |
|                                          |N30:22) * 0.0010000    |      |
|                                          +-----------------------+      |
```

Rung 2:1

The Power Demand on **Alternator A** is obtained through a Block Transfer Read from the LSM. The total power demand on Alternator A may be obtained by combining files N36:51, N36:52, and N36:53. The total power demand is in units of Megawatts and is located in file F8:1.

```
Rung 2:1
|                                          +CPT--------------------+      |
+------------------------------------------+COMPUTE                +      |
|                                          |Destination        F8:1|      |
|                                          |               637.5000|      |
|                                          |Expression             |      |
|                                          |((N36:51 * 0.0000010) +|      |
|                                          |(N36:52 * 0.0010000)) +|      |
|                                          |N36:53                 |      |
|                                          +-----------------------+      |
```

Rung 2:2

The Alternator A Bus Frequency is obtained from the LSM through a Block Transfer Read. The Alternator A Bus Frequency may be calculated by combining files N35:36 and N35:37. The frequency in Hertz is then converted into a number of digital counts (0–4095) and placed in file F8:2. The speed and power of the alternator are controlled by the number of digital counts sent to an Analog Output Module through a Block Transfer Write. The conversion factors for Hz, RPM, and digital counts are as follows:

$$\left[\frac{1Hz}{30RPM}\right] \times \left[\frac{1RPM}{2.1505\ counts}\right] = \left[\frac{1Hz}{64.52\ counts}\right]$$

```
Rung 2:2
|                                          +CPT--------------------+      |
+------------------------------------------+COMPUTE                +      |
|                                          |Destination        F8:2|      |
|                                          |               3871.200|      |
|                                          |Expression             |      |
|                                          |((N35:36 * 0.0010000) +|      |
|                                          |N35:37) * 64.52000     |      |
|                                          +-----------------------+      |
```

Rung 2:3

The total percentage of Maximum Alternator Output Power being supplied by alternator A may be calculated by dividing the Power Demand, (in Megawatts), of Alternator A (F8:1) by the Maximum Alternator Output Power, (in Megawatts), of Alternator A (F8:0) This percentage is located in file F8:3.

```
Rung 2:3
|                                                    +DIV---------------+ |
+----------------------------------------------------+DIVIDE            +-+
|                                                    |Source A      F8:1| |
|                                                    |           637.5000| |
|                                                    |Source B      F8:0| |
|                                                    |           637.5000| |
|                                                    |Destination   F8:3| |
|                                                    |             1.000000| |
|                                                    +------------------+ |
```

Rung 2:4

The “Maximum Alternator Output Power” located in files N80:22 and N80:23 is a Line Synchronization Module Factory Configuration Parameter. The calculated value in file F8:4 is **Alternator B** Maximum Output Power in units of Megawatts.

```
Rung 2:4
|                                          +CPT--------------------+      |
+------------------------------------------+COMPUTE                +------+
|                                          |Destination        F8:4|      |
|                                          |               0.000000|      |
|                                          |Expression             |      |
|                                          |((N80:23 * 1000.000) + |      |
|                                          |N80:22) * 0.0010000    |      |
|                                          +-----------------------+      |
```

Rung 2:5

The Power Demand on **Alternator B** is obtained through a Block Transfer Read from the LSM. The total power demand on Alternator B may be obtained by combining files N86:51, N86:52, and N86:53. The total power demand is in units of Megawatts and is located in file F8:5.

Continued on next page.

Load Sharing Utilizing LSM BTR Data Continued

```
Rung 2:5
|                                          +CPT--------------------+      |
+------------------------------------------+COMPUTE                +------+
|                                          |Destination        F8:5|      |
|                                          |               0.000000|      |
|                                          |Expression             |      |
|                                          |((N86:51 * 0.0000010) +|      |
|                                          |(N86:52 * 0.0010000)) +|      |
|                                          |N86:53                 |      |
|                                          +-----------------------+      |
```

Rung 2:6

The Alternator B Bus Frequency is obtained from the LSM through a Block Transfer Read. The Alternator B Bus Frequency may be calculated by combining files N85:36 and N85:37. The frequency in Hertz is then converted into a number of digital counts (0–4095) and placed in file F8:6. The speed and power of the alternator are controlled by the number of digital counts sent to an Analog Output Module through a Block Transfer Write.

```
Rung 2:6
|                                          +CPT--------------------+      |
+------------------------------------------+COMPUTE                +------+
|                                          |Destination        F8:6|      |
|                                          |               0.000000|      |
|                                          |Expression             |      |
|                                          |((N85:36 * 0.0010000) +|      |
|                                          |N85:37) * 64.52000     |      |
|                                          +-----------------------+      |
```

Rung 2:7

The total percentage of Maximum Alternator Output Power being supplied by alternator B may be calculated by dividing the Power Demand, (in Megawatts), of Alternator B (F8:5) by the Maximum Alternator Output Power, (in Megawatts), of Alternator B (F8:4) This percentage is located in file F8:7.

```
Rung 2:7
|                                                    +DIV---------------+ |
+----------------------------------------------------+DIVIDE            +-+
|                                                    |Source A      F8:5| |
|                                                    |           0.000000| |
|                                                    |Source B      F8:4| |
|                                                    |           0.000000| |
|                                                    |Destination   F8:7| |
|                                                    |           0.000000| |
|                                                    +-------------------+ |
```

Rung 2:8

Rung 2:8 allows the user to set a dead-band range where no corrective load sharing action will take place. Using file F8:8, the user can enter a small percentage to be added onto and subtracted from the total percentage of Maximum Alternator Output Power being supplied by alternator B (F8:7). The percentage of Maximum Alternator Output Power ± the user defined percentage (F8:8), will create an upper an a lower limit for a deadband range where, as seen in rungs 2:11 and 2:12, no adjustments will be made on the output power supplied be either alternator.

```
Rung 2:8
|                                                    +ADD---------------+  |
+--------------------------------------------------++ADD               ++-+
|                                                  ||Source A      F8:7|| |
|                                                  ||          0.000000|| |
|                                                  ||Source B      F8:8|| |
|                                                  ||         0.0500000|| |
|                                                  ||Destination   F8:9|| |
|                                                  ||          0.000000|| |
|                                                  |+------------------+| |
|                                                  |+SUB---------------+| |
|                                                  ++SUBTRACT          ++ |
|                                                   |Source A      F8:8|  |
|                                                   |         0.0500000|  |
|                                                   |Source B      F8:7|  |
|                                                   |          0.000000|  |
|                                                   |Destination  F8:10|  |
|                                                   |          0.000000|  |
|                                                   +------------------+  |
```

Rungs 2:9 and 2:10

Rungs 2:9 and 2:10 move the floating point values (counts 0–4095) of the bus frequencies of both alternators A and B into integer files. The number of digital counts input to the Analog Output Module will control the output of the module. Only a whole integer value of counts may be input into the Analog Output Module.

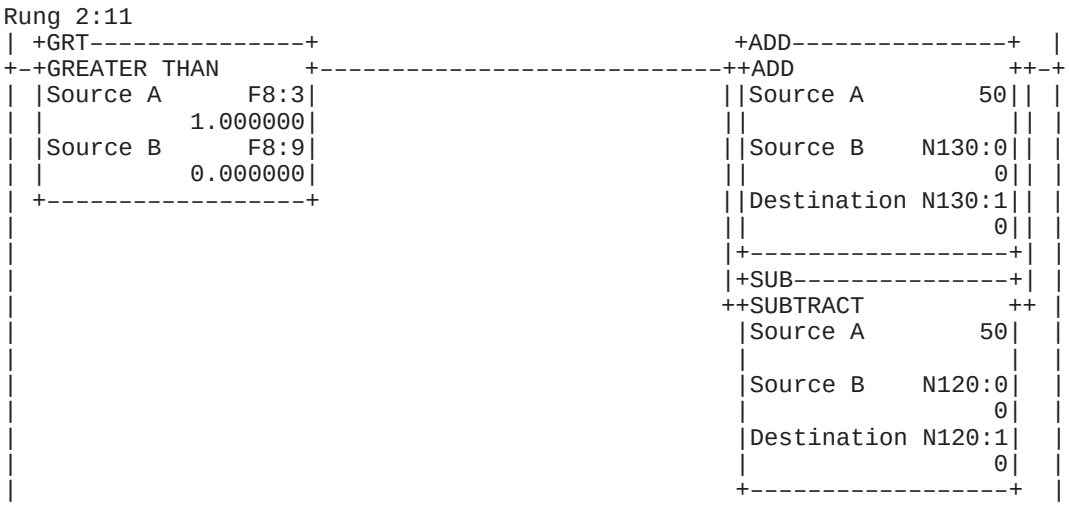
```
Rung 2:9
|                                                    +MOV---------------+ |
+--------------------------------------------------+MOVE               +-+
|                                                   |Source        F8:2| |
|                                                   |          0.000000| |
|                                                   |Destination N120:0| |
|                                                   |                 0| |
|                                                   +------------------+ |
Rung 2:10
|                                                    +MOV---------------+ |
+--------------------------------------------------+MOVE               +-+
|                                                   |Source        F8:6| |
|                                                   |          3871.200| |
|                                                   |Destination N130:0| |
|                                                   |                 0| |
|                                                   +------------------+ |
```


Continued on next page.

Load Sharing Utilizing LSM BTR Data Continued

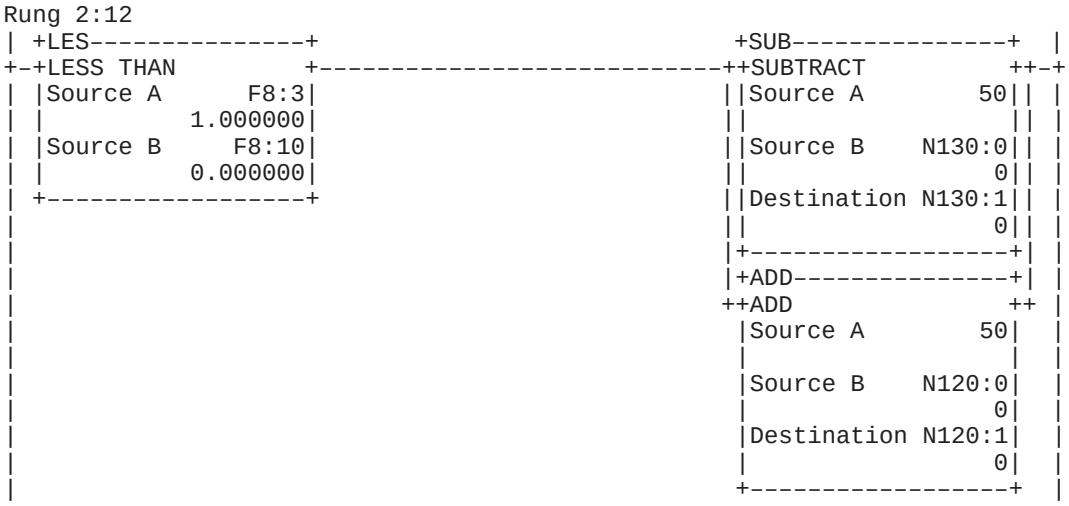
Rung 2:11

If the total percentage of Maximum Alternator Output Power being supplied by Alternator A is greater than the total percentage of Maximum Alternator Output Power being supplied by Alternator B (greater than the upper limit of the deadband range formed in rung 2:8), then raise the speed and the power of Alternator B by increasing the number of digital counts to be output to its Analog Output Module (+ 50). The speed and power of Alternator A are lowered by decreasing the number of digital counts to be output to its Analog Output Module (–50).



Rung 2:12

If the total percentage of Maximum Alternator Output Power being supplied by Alternator A is less than the total percentage of Maximum Alternator Output Power being supplied by Alternator B (less than the lower limit of the deadband range formed in rung 2:8), then lower the speed and the power of Alternator B by decreasing the number of digital counts to be output to its Analog Output Module (– 50). The speed and power of Alternator A are raised by increasing the number of digital counts to be output to its Analog Output Module (+50).



Rung 2:13 and 2:14

Load Sharing corrections may only be made if input I:00/0 is set. All load share calculations will continually be made, but the corrected output speeds for each of the alternators will not be written to the Analog Output Module until input I:00/0 is toggled from OFF to ON. Rung 2:13 is the BTW for alternator A, and rung 2:14 is the BTW for alternator B.

```
Rung 2:13
| I:000                                  +BTW--------------------+      |
+--] [----------------------------------+BLOCK TRANSFER WRITE   +-(EN)-+
|    00                                  |Rack                 00|      |
|                                        |Group                 2+-(DN) |
|                                        |Module                0|      |
|                                        |Control block    N150:0+-(ER) |
|                                        |Data file        N120:1|      |
|                                        |Length               13|      |
|                                        |Continuous            N|      |
|                                        +-----------------------+      |
Rung 2:14
| I:000                                  +BTW--------------------+      |
+--] [----------------------------------+BLOCK TRANSFER WRITE   +-(EN)-+
|    00                                  |Rack                 00|      |
|                                        |Group                 3+-(DN) |
|                                        |Module                0|      |
|                                        |Control block    N160:0+-(ER) |
|                                        |Data file        N130:1|      |
|                                        |Length               13|      |
|                                        |Continuous            N|      |
|                                        +-----------------------+      |
Rung 2:15
|                                                                       |
+----------------------------[END OF FILE]-------------------------------+
|                                                                       |
```

Rockwell Automation

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