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Allen-Bradley
Latching (10-27V DC) Input Module

(Cat. No. 1771-DS)

Product Data

Description

The Latching (10-27V DC) Input Module detects and latches pulses of 0.1 to 5.0 ms duration. When the module detects a pulse at an input terminal, it sets a bit in the corresponding input image table address on the next I/O scan.

Input Device

The latching input module responds to pulses from optical sensors that have:

- isolated pulse outputs
- isolated gate outputs

The off-state leakage current of your optical sensors should not exceed 1mA @ 4V DC.

Input Operation

The module's inputs operate in either of two ways:

- Independent: each input operates independently unless paired
- Paired: one input responds to a gate signal, the other responds to a pulse

Independent Inputs

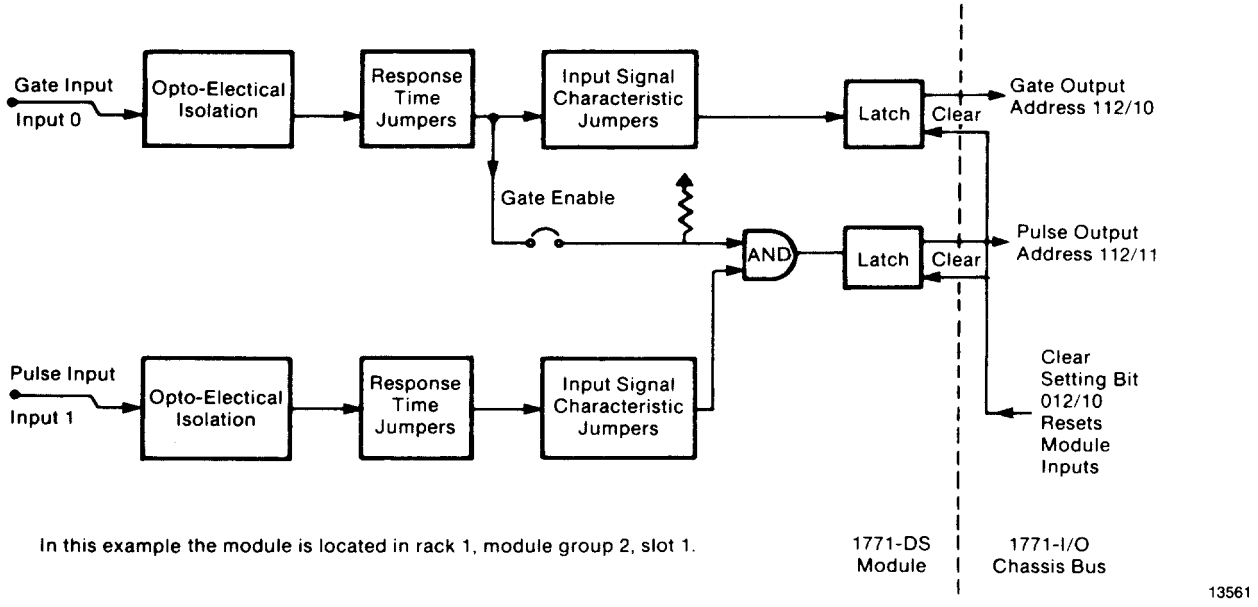
Use independent inputs for detecting pulses in a single-pulse environment.

Paired Inputs

Use paired inputs when your application requires detecting selected pulses in a multi-pulse environment. You can select up to four paired inputs per module. When using paired inputs, the module must detect a gate signal in order to detect and latch a pulse input. The module "ands" the pulse and gate inputs in order to latch the pulse (figure 1) Typically, gate signals and pulses are generated by separate optical sensors.

Refer to Selecting Module Functions for the method of selecting input operation.

Figure 1
Latching Input Module Block Diagram



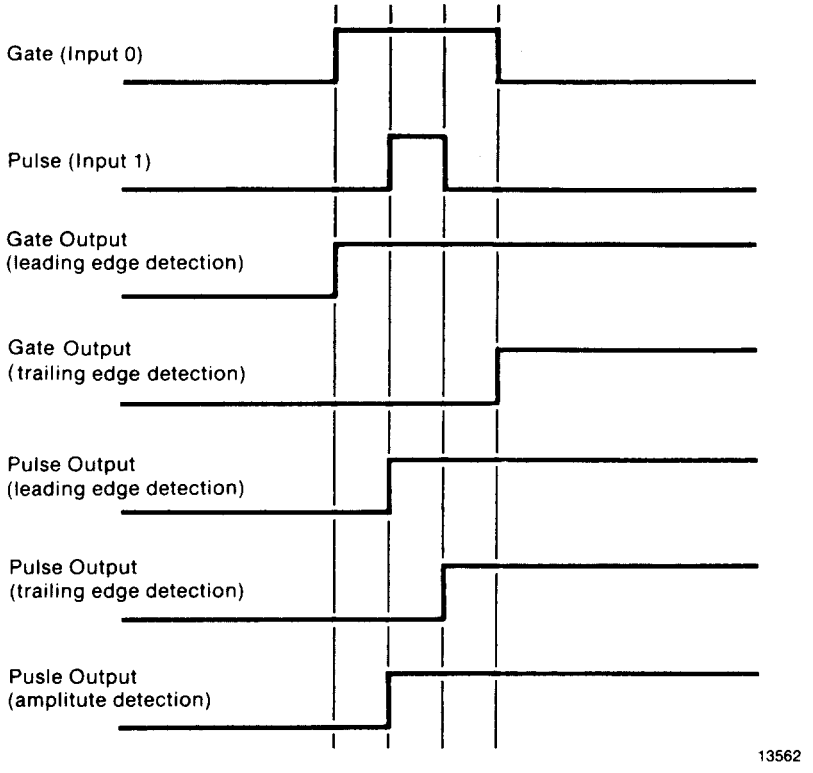
Pulse Detection

The module's inputs, whether independent or paired, can respond to a pulse's leading or trailing edge, change in state, or amplitude triggering (level detection.) Amplitude triggering allows the module to detect the presence of a pulse independent of your choice of leading or trailing edge detection. You select the type of detection for each input independently.

Selecting Pulse Detection for Paired Inputs

Select leading or trailing edge detection if pulses will always occur within the duration of the gate signal. Timing diagrams of the module's response to a pulse and gate signal under this condition are shown in figure 2.

Figure 2
Module Response to a Gate Signal and Pulse when Pulse appears within Gate



Select amplitude triggering when pairing inputs, or when the pulse could rise or fall ahead of and/or following, respectively, the gate signal's leading or trailing edge. This includes pulses of longer duration than the gate signal (figure 3). Timing diagrams for the pulse leading (but overlapping) the gate signal are shown in figure 4. Timing diagrams for the pulse trailing (but overlapping) the gate signal are shown in figure 5.

Refer to Selecting Module Functions for the method of selecting pulse detection.

Figure 3
Example of a Pulse input preceding, following, or overlapping the Gate Signal

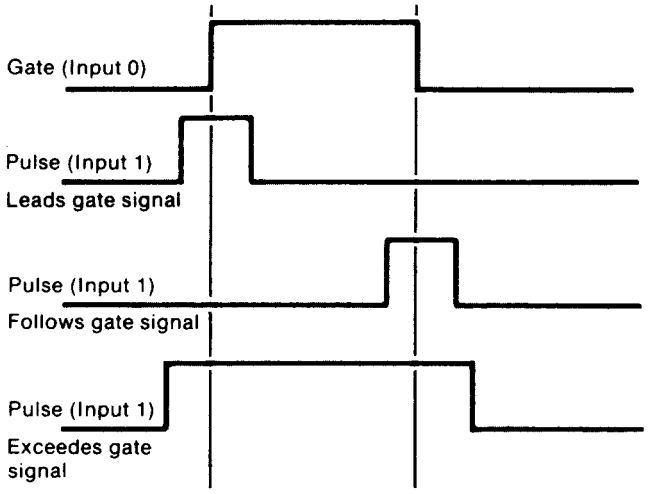


Figure 4
Module response to a Pulse that precedes the Gate Signal

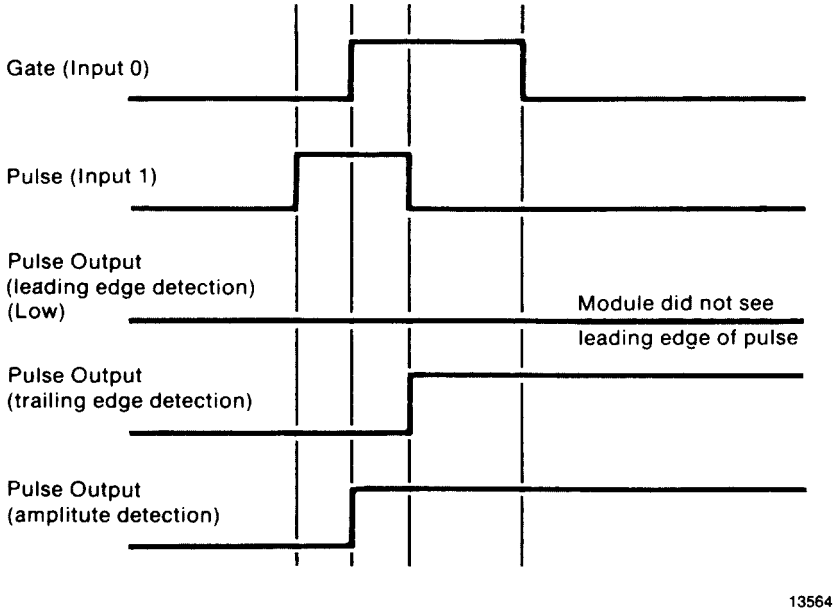
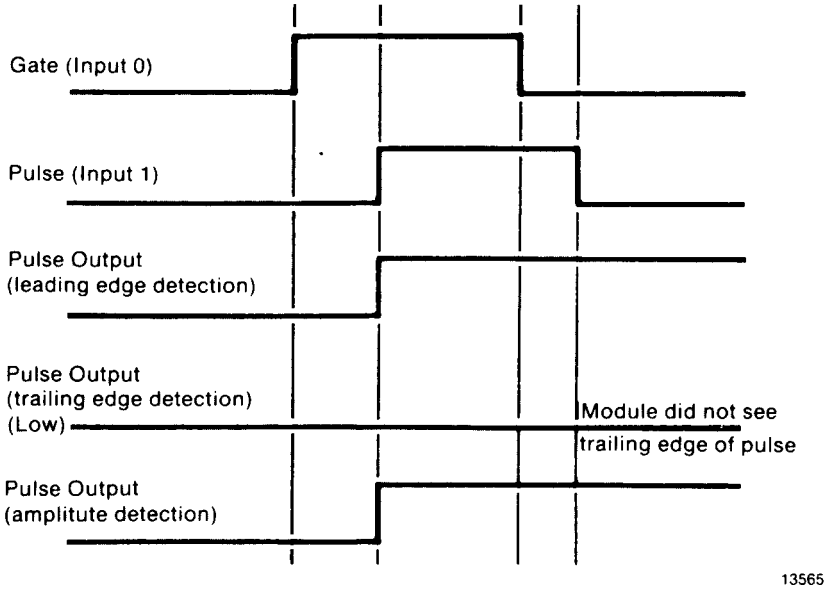


Figure 5
Module response to a Pulse that trails the Gate Signal



Pulse Capture Time

The pulse capture time is the minimum pulse width that the module will capture. You can select any one of the following pulse capture times for each input:

0.1ms, 0.5ms, 1.0ms, 2.5ms, or 5.0ms

Select the pulse capture time after measuring the duration of typical input pulses and the duration of any electrical noise pulses. Use the following relationship for choosing the pulse capture time:

Electrical Noise	$<$ Pulse Capture Time	$\leqslant$ Pulse Time

Refer to Selecting Module Functions for the method of selecting pulse capture time. When pairing inputs, refer to Timing of Paired Inputs.

Recovery Time

The module requires time to recover after each pulse. The recover time between pulses depends on the pulse capture time that you select as follows:

Selected Pulse Captured Time (ms)	Time Between Pulses (ms)
5	25
2.5	12.5
1	5
0.5	2.5
0.1	0.5

Capture Time (Paired Inputs)

We recommend that you select the shortest usable capture time for the gate and pulse when using paired input. This reduces lag time in the module. Set the gate and pulse capture times to the same value. Unequal values may prevent the module from operating correctly if timing considerations (figure 6) are not met.

Timing Of Paired Inputs

Three timing relationships that you should consider when using paired gate and pulse inputs are:

- Guaranteed pulse detection - pulse within the gate
- Guaranteed non-detection of pulse - pulse outside gate
- Minimum time between gates

Pulse and gate signals are delayed in the module. The delay between pulse and gate signals that allows a margin of safety to guarantee detecting or non detecting a gated pulse is the pulse capture time. We designate this timing margin M.

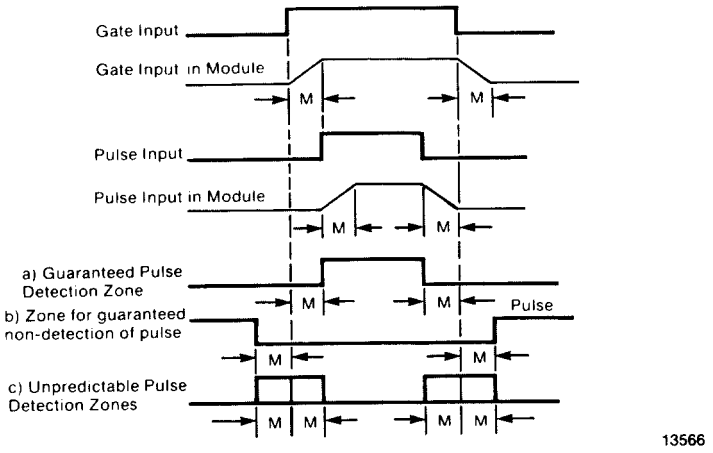
Guaranteed Detection The module detects a pulse when the pulse turns on after the gate turns on by M (leading edge of the pulse lags the leading edge of the gate by M); and the pulse turns off before the gate turns off by M (training edge of the pulse precedes the trailing edge of the gate by M). (figure 6a)

Guaranteed Non-detection The module cannot detect a pulse when the pulse turns off before the gate turns on by M (trailing edge of the pulse precedes the leading edge of the gate by M); and the gate turns off before the pulse turns on by M (trailing edge of the gate precedes the leading edge of the pulse by M). (figure 6b)

Upredictablity Zones Pulse detection is unpredictable under the following circumstances (figure 6c):

Type of Pulse Detection	Unpredictability Zone
leading edge	leading edge of pulse is within ± M of the leading edge of gate
trailing edge	trailing edge of pulse is within ± M of the trailing edge of gate
amplitude detection	pulse is within ± M of the leading or trailing edge of gate

Figure 6
Timing Of Paired Gate and Pulse inputs



Minimum Gate Width The width of the gate must exceed twice the pulse capture time, M, that you select. For example, if the minimum gate width from your optical sensor exceeds 1ms, set your pulse capture time to 0.5ms or less.

Electrostatic Discharge

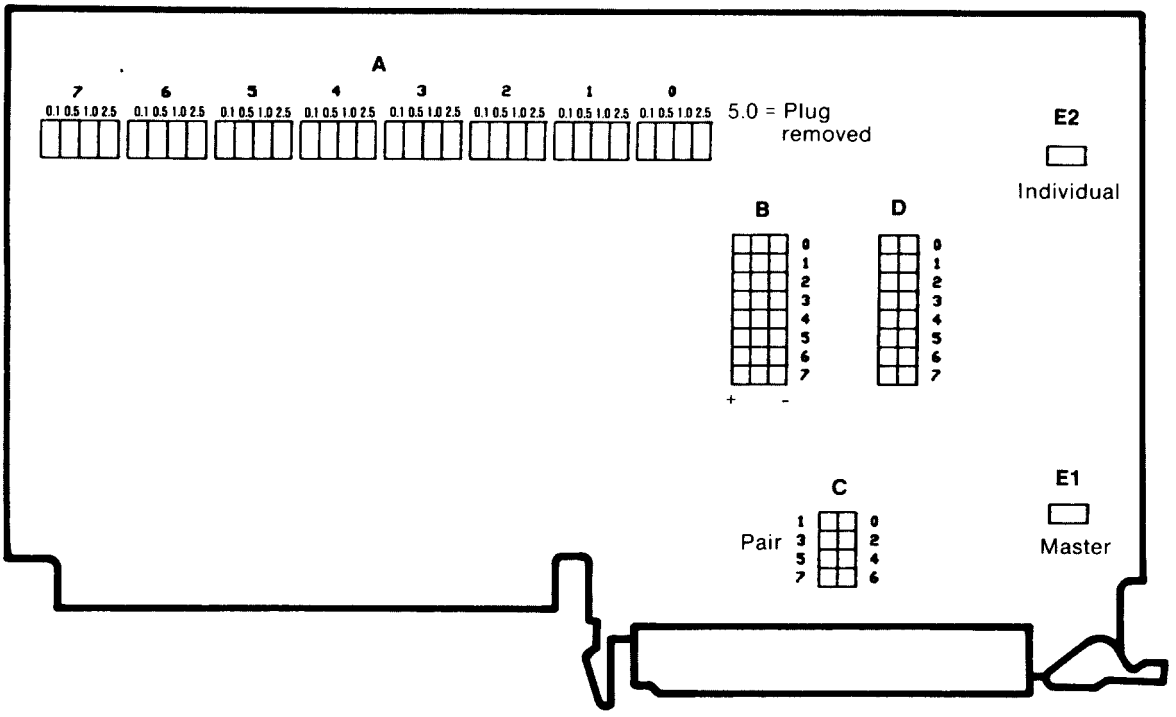
Under some conditions, electrostatic discharge can degrade performance or damage the module. If you observe the following precautions you can guard against electrostatic damage.

- Touch a grounded object to discharge yourself before handling the module.
- Do not touch the backplane connector or connector pins.
- When you configure or replace internal components, do not touch other circuit components inside the module. If available, use a static-safe work station.
- When not in use, keep the module in its static-shield bag.

Selecting Module Functions

You select module functions by placing configuration plugs (jumpers) on appropriate pairs of pins. First, remove the module's cover by removing the four corner screws. Then, locate jumper zones A thru E on the printed circuit board (figure 7), and set the jumpers according to your application requirements. Store unused jumpers by placing them on only one pin of the pair so the jumper is electrically floating.

Figure 7
Locations of Jumper Zones A thru E and Jumper Settings



A PULSE CAPTURE TIME (1 PLUG/CHNL)
Insert plug for minimum channel capture time.
Remove plug for 5ms minimum capture time.

B EDGE DETECTION (1 PLUG/CHNL)
Insert plug at (-) for trailing.
Insert plug at (+) for leading
Remove plug for change of state.

C PAIRED/INDEPENDENT INPUTS
Insert plugs for paired inputs.
Remove plugs for independent inputs.

D LEVEL DETECTION
Insert plugs for level detection,
otherwise remove plug.

E RESET (one plug only)
E1 - Insert plug for all channels simultaneously or
E2 - Insert plug for each channel individually.

Note: Numbers 0 thru 7 are input channels.
Store removed plug on single pin.

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Programming

Use immediate input instructions to reduce the time required by the processor to read latched inputs from the module. You should move latched inputs to storage locations each scan, and avoid writing new data over old data before using it. Block transfer is not used.

Reset

You can reset the module's latched inputs in either of two ways (figure 7).

If you choose	Then
Master	all inputs are reset together
Individual	each input is reset individually

Your program logic an reset individual inputs or can reset all inputs in one scan according to the reset mode that you select. The processor sets data table bit(s) corresponding to the latched input(s), then resets the module's input(s) in the same scan.

You reset individual inputs by setting the corresponding bit in the module's output image table word address. For example, you reset terminal 4 of a module in rack 1, module group 2, slot 1 by setting output image table bit 012/14.

If you have selected module reset, your program logic can reset all eight module inputs at once. It does this by setting the least significant bit in the module's output image table word address. For example, you reset a module located in rack 1, module group 2, slot 1 by setting output image table bit 012/10.

WARNING: Do not use the complementary address of this module for other purposes, or any I/O module as the complement to this module. The complementary word address must be reserved for the reset function. If you use the complementary address for purposes other than resetting the module, unpredictable operation could occur with possible damage to machinery and/or injury to personnel.

Reset Considerations

For your module to operate correctly, the time required to reset a latched input must be less than the time between pulses. This is important when attempting to detect rapid pulses when your module is in a remote I/O chassis.

To reset a latched input, your program must toggle (reset then set) the corresponding output bit. If the module captures another pulse during the toggle period (program scan plus two remote I/O scans), the processor does not detect the subsequent latched input(s). To detect these inputs, reduce program and/or remote I/O scans so that the toggle period is less than the time between pulses.

We recommend that you use one or more of the following methods:

- Repeat the reset logic in your ladder program to reduce program scan time.
- Use a real time interrupt to reset the module's inputs at a rate faster than the pulse rate you wish to detect.
- In a remote system, place the I/O chassis containing the module on a processor channel having no other assigned rack numbers.
- If you are using a PLC-2 family processor in a local configuration, use immediate input and output instructions to reduce program scan time.

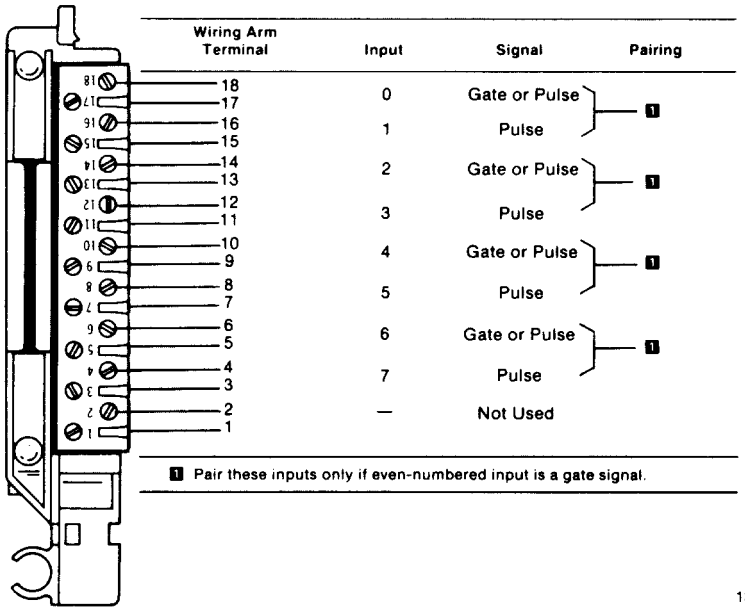
Input Indicators

Eight status indicators are located on the front of the module to show the status of inputs. These indicators are useful when troubleshooting or when initially installing the module and its input devices. The status indicator for an input lights when the input is latched.

Field Wiring Arm

Connect wires from your input devices to the 1771-WF 18-terminal field wiring arm (figure 8). Attach it to the 1771 I/O chassis so that it can pivot upward to connect quickly and conveniently with connections on the front of the module. The wiring arm allows you to easily remove an I/O module without rewiring.

Figure 8
Field Wiring Arm Connections



WARNING: Remove power from the 1771I/O chassis backplane and wiring arm before removing or installing an I/O module.

- Failure to remove power from the backplane or wiring arm could cause module damage, degradation of performance, or injury.
- Failure to remove power from the backplane could cause injury or equipment damage due to possible unexpected operation.

Input Connections

You can connect the module's inputs either as a current source (figure 9) or as a current sink (figure 10). The module's inputs are protected from the application of reverse voltage up to 240V DC.

Figure 9
Typical Current Source Connections

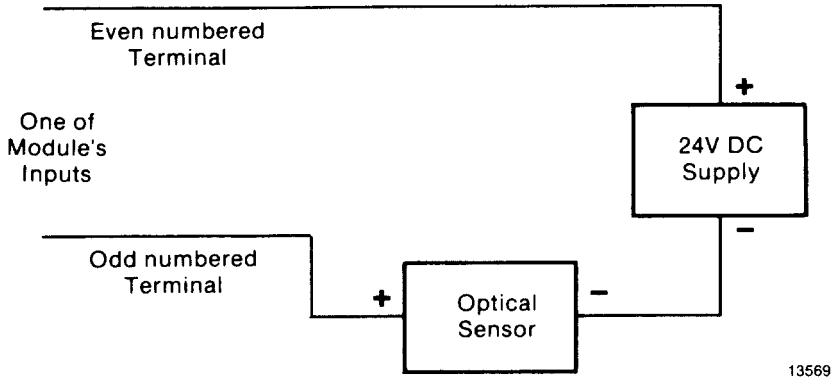
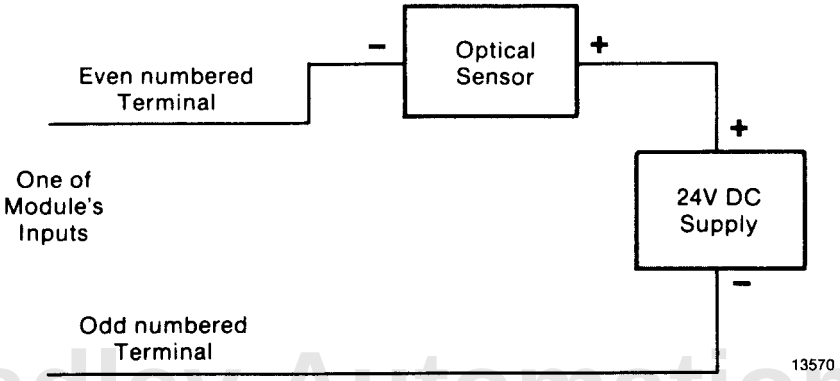


Figure 10
Typical Current Source Connections



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Latching (10-27V DC)
Input Module

Keying

The module is keyed to guard against installation in the wrong module slot. To implement this protection, insert keying bands supplied with your I/O chassis into the upper backplace connector of the slot for this module in the following positions.

Between 2 and 4
Between 18 and 20

You can change the positions of keying bands of subsequent system design requires the insertion of a different type of module in this slot.

Specifications

Inputs
- 8

Module Location
- 1771 I/O chassis

Pulse Capture Time
- 0.1, 0.5, 1.0, 2.5, or 5.0ms

Input Voltage Range
- 10 to 27V DC for a logic 1
- 0 to 4V DC for a logic 0

Reverse Voltage Protection
- 240V DC max

Maximum Off-State Current
- 1mA @ 4V DC

Nominal Input Current
- 20mA @ 27V DC typical

Opto-Electrical Isolation
- 1500V

Backplane Current
- 375mA typical

Environment Conditions
- Operating Temperature
  0 to 60°C (32 to 140°F)
- Storage Temperature
  40 to 85°C (-40 to 185°F)
- Relative Humidity
  5 to 95%
  (without condensation)

Keying
- Between 2 and 4
- Between 18 and 20

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