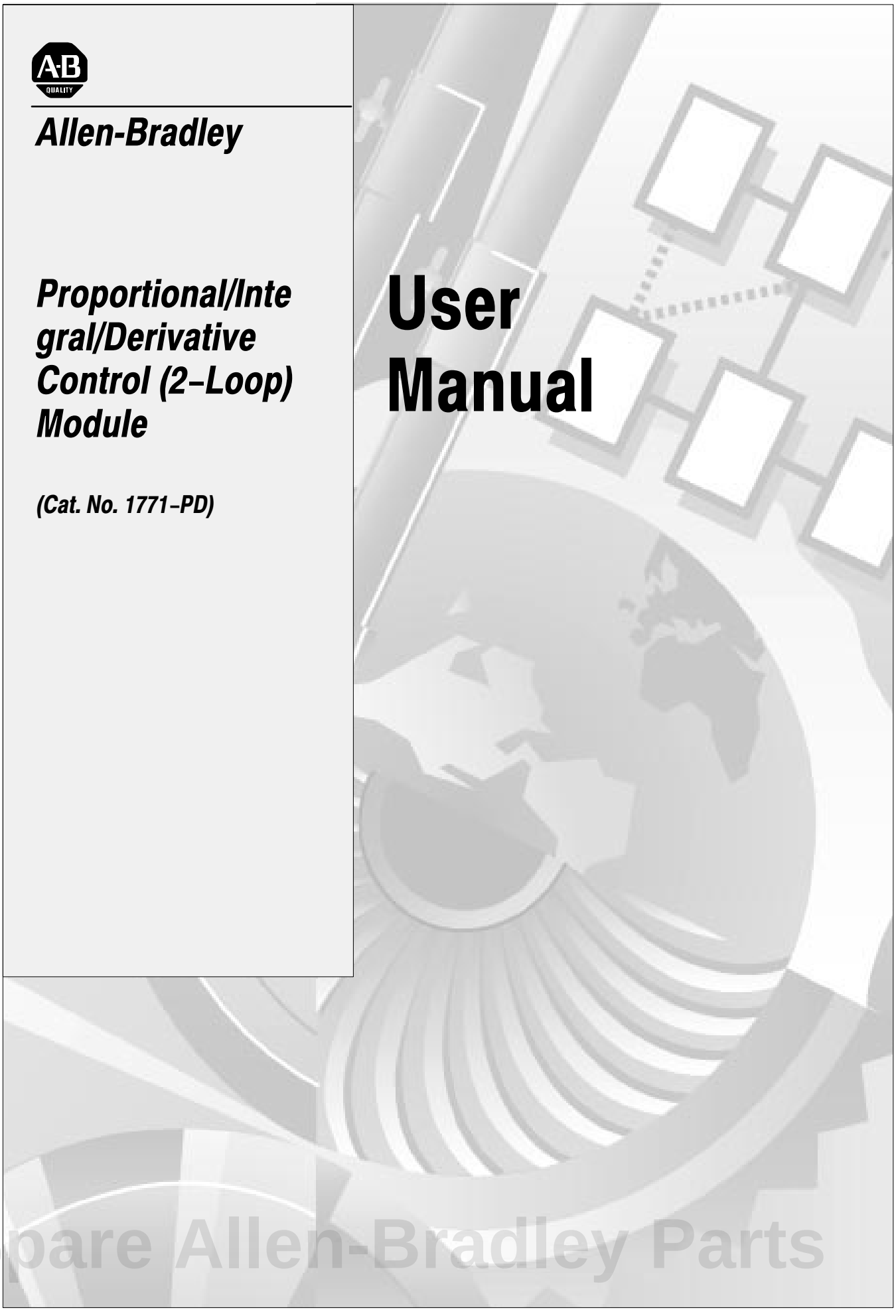


Allen-Bradley

Proportional/Integral/Derivative Control (2–Loop) Module

(Cat. No. 1771–PD)

User Manual

Table of Contents

Chapter 1

Introduction

General

The Proportional/Integral/Derivation Control (2-loop) Module Assembly (cat.no.1771-PD) is an intelligent I/O module that performs closed loop PID control. The PID module is a process controller. The PID module monitors the analog input process variable, compares the input to the desired set point, and calculates the analog output control variable based on the control algorithm programmed in the module. The PID module has the hardware inputs and outputs and microprocessor to perform PID control.

The PID module assembly consists of:

- 1 Proportional/Integral/Derivation Control (2-loop) Module (cat. No. 1771-PD)
- 1 Field Wiring Arm (cat. No. 1771-WF)

The PID module can control up to two closed loops such as flow, temperature, pH, and level. Advanced control features include cascade, feedforward, scaling, square root, error squared, digital and led/lag filtering. The PID module can directly interface with an optional user supplied manual control station. Transition from manual to automatic control can be performed with bumpless transfer.[1] Input and output ranges can be selected for each loop to either +1 to +5V DC or +4 to +20mA.

The PC processor uses block transfer programming to communicate with the module. The PC processor writes loop configuration parameters such as gain constants, set points, digital filter values, limits, alarm points to the PID module and reads status information such as analog input values, analog output values, limit alarms and diagnostics from the PID module. The PID module can be used with any Allen-Bradley PC processor that has block transfer capability and uses the 1771 I/O structure.

When using the Mini-PLC-2 and PLC-2/20 processors, programming will be more lengthy because these processors do not have the block format instructions which permit shorter programs and easier data monitoring.

[1] Bumpless transfer, as defined in Fundamentals of Process Control Theory by Paul W. Murril, means a smooth transition from manual to automatic control.

Capabilities

The PID module can control one or two PID closed loops. The two loops can be independent or linked together by and advanced control function such as cascade or decoupling. Expanded loop features can be chosen in addition to standard features to suite the application. All features are software selectable with the exception of the I/O range, the source of +5V DC, and the fault response to a hardware failure (which are selected using internal programming plugs). Write block transfers to the module allow program logic to enable the following features:

Standard features for input conditioning

- detect the loss of process variable input
- read the process variable at the PC processor
- substitute a value from the PC processor for the process variable
- take the square root of the process variable
- \\digitally filter the process variable

Standard control features

- select direct or reverse acting control
- download a set point from the PC processor
- limit and/or set an alarm on the error signal
- download a dead band value from the PC processor
- perform error dead band (zero crossing)
- set an alarm when the error exceeds the dead band
- select the control mode: proportional only, integral only, proportional and integral, proportional and derivative, or all three
- select error or error squared conditioning of the proportional and/or integral error
- select whether the derivative function operates on the error or the process variable
- set an alarm on the proportional term
- limit and/or set an alarm on the integral term
- limit and/or set an alarm on the derivative term

Standard features for output conditioning

- limit and/or set an alarm on the PID algorithm output
- read the PID algorithm output at the PC processor
- download an output value from the PC processor
- interface directly with a manual control station (bumpless transfer)
- hold the PID algorithm output for independent loop tuning
- hold the bias/feed forward term for independent loop tuning

- download an output bias from the PC processor

Expanded control features

- perform scaling on the process variable, set point and/or error
- set minimum and maximum scaling values
- use the tieback as the feedforward input
- take the square root of the feedforward input
- add a feedforward offset
- multiply the feedforward term by a constant
- perform lead/lag filtering on the feedforward term
- download a feedforward value from the PC processor
- cascade the output of loop 1 into the set point of loop 2
- decouple the VPID output of loop 1 into the feedforward input of loop 2

These features including integral term anti-reset wind-up are described in chapter 3.

PID Algorithm

An algorithm is a step-by-step procedure. The purpose of the PID algorithm is to maintain the process at the desired setpoint. A diagram of PID closed loop control is shown in Figure 1.1a.

The PID module has many features. Select only those features that are required for the particular application. Major control functions are shown in Figure 1.1b. Refer to figure 3.15 for a detailed algorithm flow chart. This flow chart shows the relationship of the user-selectable features.

PID modules (rev C or later) let you select the ISA or Allen-Bradley algorithm. Refer to appendix E for a comparison of algorithm values.

Hardware Description

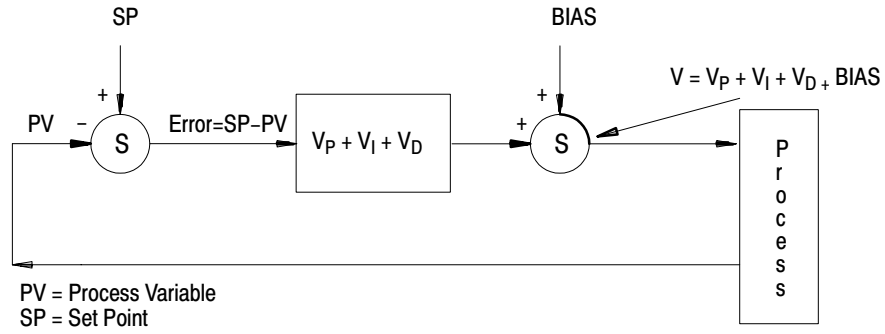
The PID module has four analog inputs and two analog outputs each with 12-bit binary resolution. Each input and output can be individually selected to either the +4 to +20mA or +1 to +5V DC range without recalibration. The selection is made with internal programming plugs. Each loop has one process variable input, one tieback input and one analog output associated with it. The tieback analog input is used to track the analog output of the manual control station to permit bumpless transfer. Each loop uses one discrete input to track the status of the optional manual control station. A contact output is used to switch the

manual control station of both loops to manual control. The module's analog inputs can be read and outputs can be set by the PC processor.

The PID module can draw its +5V DC operating power from either the chassis backplane power supply or from a user-supplied +5V DC power supply through the field wiring arm. The external power supply option permits a more fault tolerant system by allowing the PID module to be powered independently. The PID module also requires +15V DC power for the analog circuitry.

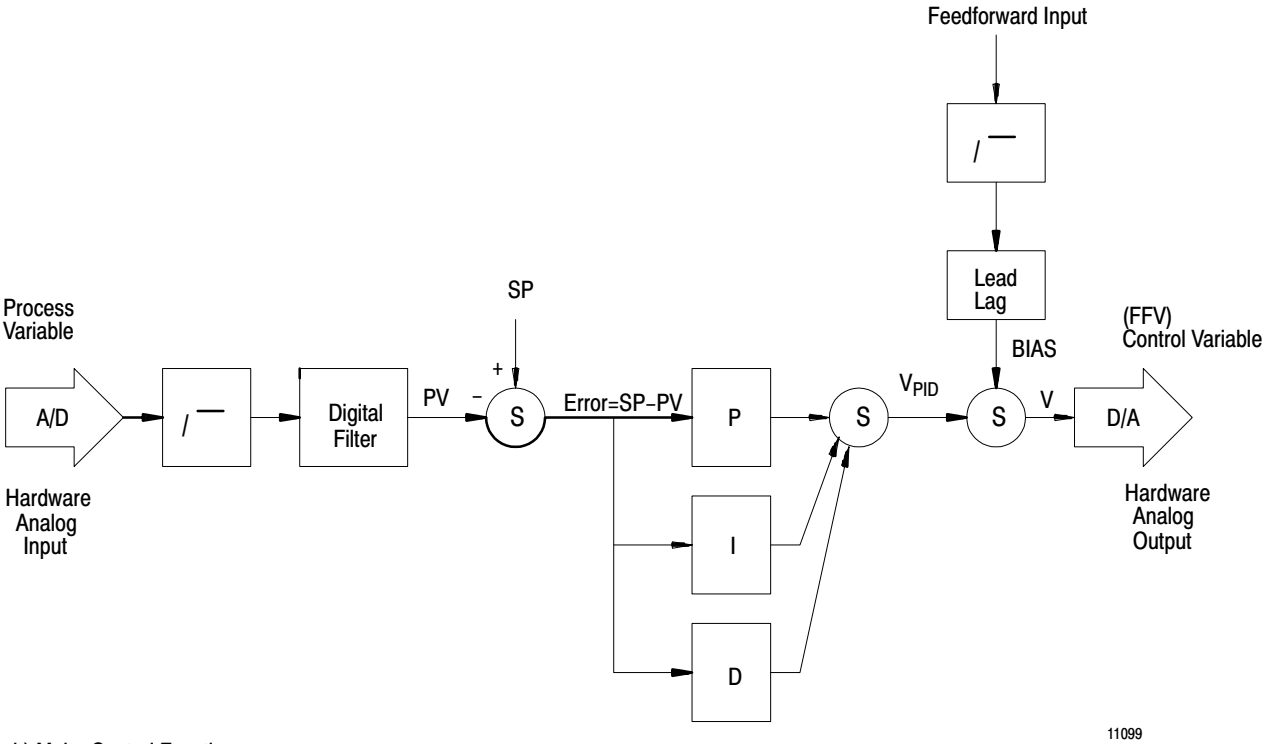
Typical PID hardware and signal paths are shown in Figure 1.2.

Figure 1.1
Simplified PID Algorithm



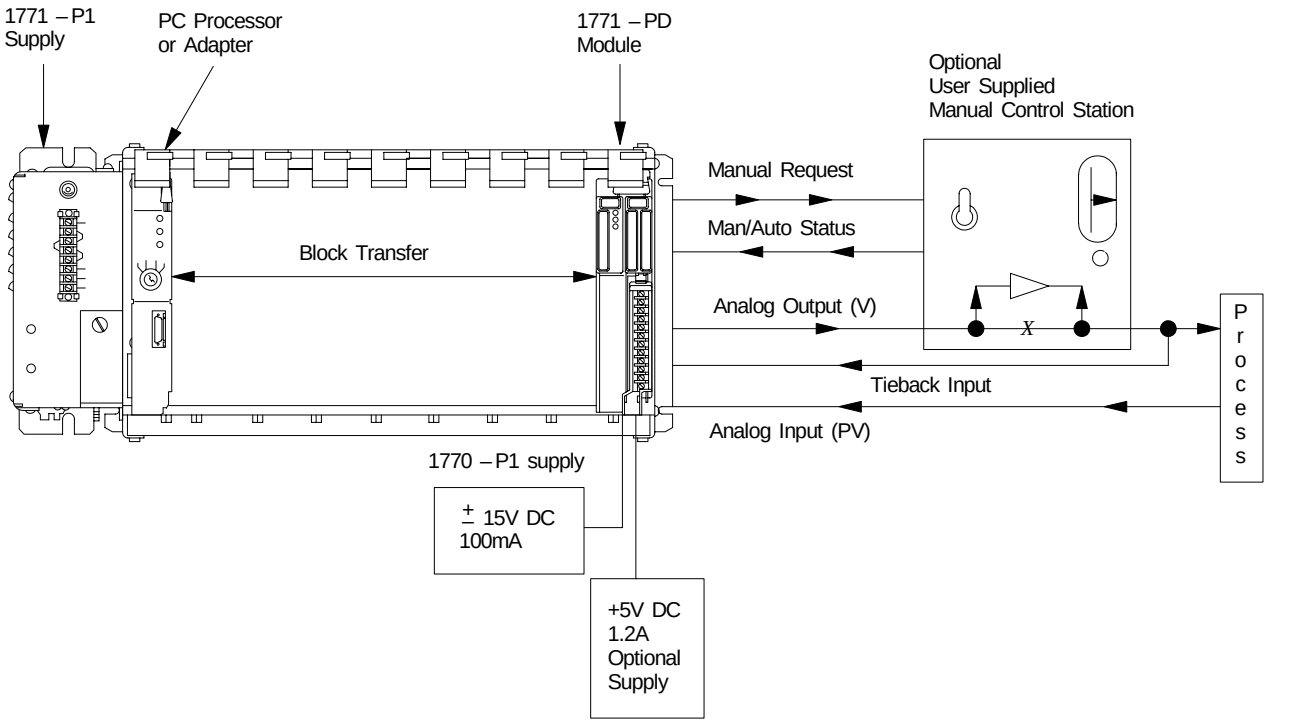
A-B	ISA
V = Control Variable	Control Variable
V_P = Proportional Term K_P	Controller Gain K_C
V_I = Integral Term K_I	Reset Term $1/T_i$
V_D = Derivative term K_D	Rate Term T_d

a) PID Closed Loop Control



b) Major Control Functions

Figure 1.2
System Overview



Programming Description

The PID algorithm can be adapted to the particular control application by selecting desired features. The features and parameter values are chosen and stored in the PC processor data table. The PC processor transfers to the PID module data table blocks which contain the feature selections and parameter values. The module uses the values to establish its operational characteristics. The PC processor can read the module status by transferring information from the module into the data table. Communication between PC processor and PID module is performed by block transfer programming.

Levels of Fault Tolerance

The module has five levels of fault tolerance.

The first level occurs when the PID module is operating properly but a loss of communication with the active PC processor occurs. The module enters a mode of operation defined as soft fault. A soft fault occurs when:

- PC processor operation is changed from run mode to program or test mode
- a PC processor fault occurs
- a communications cable break occurs between the PC processor and the I/O chassis

Each loop can be programmed independently to one of the following responses when a soft fault occurs:

- set the analog output to minimum value (+4mA or +1V DC)
- holds the analog output to the last value before the soft fault occurre
- performs PID control based on the last values transferred to the module before the soft fault occurred.
- sets the analog output to maximum value (+20MA or +5V DC)

The second level of fault tolerance is how the module sets its outputs in response to a hard fault. A hard fault occurs when the module detects a failure of its microprocessor or its self-diagnostics. Internal programming plugs are used to select the manner in which the PID module can respond if a hard fault should occur:

- sets analog output to minimum value (+4MA or +1V DC)
- holds analog outputs at the last value before the fault occurred
- sets analog outputs to maximum value (+20mA or +5V DC)

Note: These hard fault responses cannot be ensured if a component in the analog output circuit should fail.

A manual control station can be connected between the PID module analog output and the controlled element of the process. Control of the output can be switched manually to the manual control station by a switch at the station. Manual control at the station overrides the PID module's output.

The third level of fault tolerance is automatic switching of control to the manual control station when a hard fault occurs. A relay contact in the PID module closes automatically (manual request), putting the station in control. The module's output is overridden by the station output.

The fourth level of fault tolerance is the module's response to loss of +5V DC. Outputs respond as if a hard fault occurred (a or C above, but not b). The same programming plug configuration selects the module's response. If +15V DC is lost, analog outputs go to minimum value, regardless.

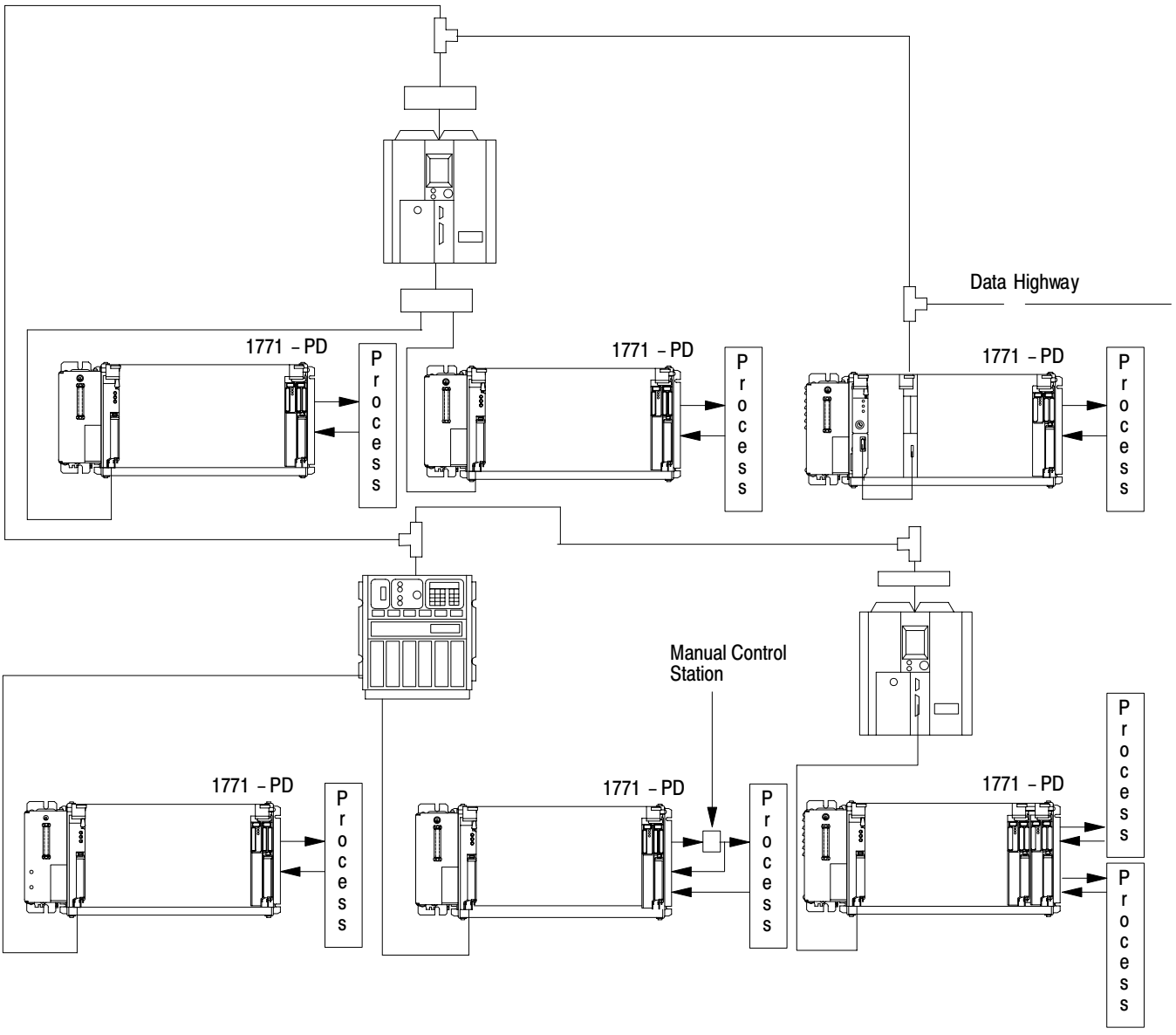
The last level of fault tolerance results from powering the module from external +5V DC and ± l5V DC power supplies, independent of I/O chassis backplane power, through the field wiring arm.

Application in Control Systems

The PID module performs closed loop control. Once programmed, it can operate independently of the PC processor. System status and alarm information can be reported to the PC processor to ensure safe system performance.

Redundant control is another alternative. PID modules could serve as back-up to a PC processor performing the PID loop algorithms. The PC processor can control many complex and interaction loops using PID modules for analog inputs and outputs. The complex algorithm could be subdivided into individual loop algorithms stored in the PID modules operating as analog I/O modules. In the event of a PC processor failure or loss of communication between PC processor and a PID module, the soft fault mode of the PID module would allow it to automatically control its loops according to the PID loop algorithms stored in its memory if the appropriate soft fault response had been selected.

Figure 1.3
Levels of Distributed Control



The PID module can also be used in a system with adaptive control based on the PC processor's ability to constantly adjust the control algorithm in the module.

Finally, PID modules can be used in distributed control schemes. The data highway can be used to link PC processors which are controlling PID modules. Figure 1.3 shows the various levels of distributed control.

Manual Overview

The remainder of the manual explains different aspects of PID module operation.

- Chapter 2 - Assembly and Installation contains hardware information including wiring diagrams, programming plug selection of I/O ranges and compliance, installation and keying, wiring diagrams and specifications of the PID module and power supplies.
- Chapter 3 - Programming contains detailed explanations of all the software selectable features.
- Chapter 4 - Troubleshooting contains helpful troubleshooting information.
- Chapter 5 - Calibration presents the procedure for recalibrating the PID module.
- Appendix A contains recots which are helpful when selecting features and programming the module.
- Appendices B and C provide sample ladder diagram programs based on sample applications.
- Appendix D contains summaries of value words and control bits used when programming.
- Appendix E shows how to convert ISA standard values to 1771-PD gain values.
- Appendix F is an enlarged algorithm flow chart for your convenience.

Chapter 2

Assembly and Installation

General

The PID module must be configured internally and wired externally to suite the conditions under which the module will be used. Module and power supply specifications are listed at the end of this chapter.

Hardware Description

The PID module is a dual-slot module. The left front panel contains three LED indicators, the right front panel contains a write-on label that can be used to record the voltage or current range and the most recent date of calibration. An 18 terminal field wiring arm is connected to the lower right front of the module for I/O and power connections. The label on the right cover plate identifies the terminals of the field wiring arm.

Diagnostic Indicators

Front panel indicators (Figure 2.1) allow an operator to observe the operating condition of the module. The indicators will be on, off or flashing (Table 2.A).

Figure 2.1
Diagnostic Indicators

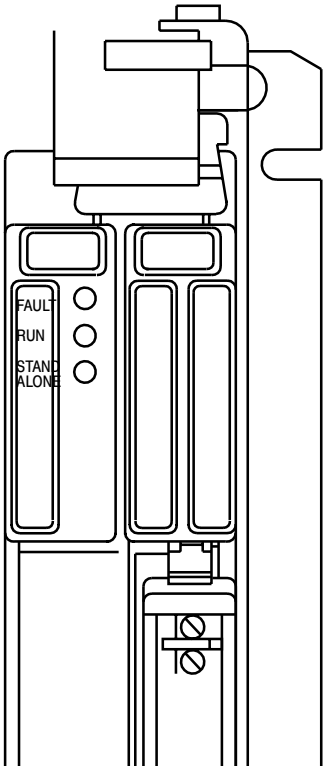


Table 2.A
Indicator Diagnostics

Indicator	State	Condition
FAULT (red)	OFF	Normal operation.
	ON	Hardware fault. Analog outputs are held at either last state, minimum or maximum value as determined by the user-selected programming plugs. If this indicator is on, the other indicators are not valid
RUN (green)	ON	Normal operation
	Flashing	PID module is initially powered (unprogrammed and is waiting for data from the PC processor.
	OFF	PID module is not in the normal run mode.
	Toggle	Analog power (±15V dc) is lost when STAND ALONE and RUN indicators are alternately toggling on and off.
STAND ALONE (yellow)	OFF	Normal operation
	Flashing	The module is in soft mode and is controlling PID loops independently. It is not communicating with an active PC Processor. NOTE: Disconnecting the field wiring arm will interrupt PID control.
	Toggle	Analog power (±15V dc) is lost when STAND ALONE and RUN indicators are alternately toggling on and off.
	ON	A programming error is causing a block transfer communication error.
NOTE: All indicators are off when in calibration mode.		

Internal Selections

In order to accommodate a wide variety of applications, a number of programming (jumper) plugs must be correctly positioned inside the PID module. The following functions are user-selectable using the programming plugs:

output range: +4 to +20mA or +1 to +5V dc
input range: +4 to +20mA or +1 to +5V dc
tieback input range: +4 to +20mA or +1 to +5V dc, if used current
output compliance: standard or additional hard fault output: hold last value or max/min value output for loss of +5V dc: max or min value
+5V dc source: backplane or external

Calibration of the I/O ranges should be checked yearly to maintain specified accuracy.

Programming Plugs and Locations

The PID module contains two printed circuit boards. The left-hand board is the digital board, the right-hand board is the analog board.

Programming plugs are located on both the analog and digital circuit boards inside the PID module. Typically they stand higher than the surrounding components on the circuit board. The programming plug locations are labeled E1 through E24 on the analog board. The only user-selectable programming plugs on the digital board are E2 and E10.

Some of the programming plug locations are factory configured and must remain in the configuration except during calibration. They are called out as factory configured in the programming plug position tables and in the figures which show their locations.

User-selectable plug locations have either two or three pins per plug. Programming plugs electrically connect two pins. The plug can be placed over the required pins or stored by placing the plug over a single pin, electrically floating.

Programming Plug Selection

Programming plugs should be set with care after decisions are made which govern their placement. The following procedure will be helpful to ensure that all the programming plugs are properly set. The procedure consists of 5 parts.

a. Select digital board features. Record features on Table 2.B

b. Select analog board features. Record features on Table 2.C.

c. Record the position on analog plugs by completing Table 2.D.

d. Set programming plugs on the digital board using Table 2.B.

e. Set programming plugs on the analog board using Table 2.D.

Selection Procedure (Part A)

Begin with digital board features using Table 2.B.

1. The hard fault response of the module is selected first. A hard fault occurs when a module failure is detected in the event of a failure, the analog output will either maintain the last value or will be set to the minimum or maximum value. A single choice is made for both outputs as to whether they hold last value or go to minimum/maximum.

Select hold last value or go to minimum/maximum for the hard fault response. Record your selection on Table 2.B by circling RIGHT for hold last value or LEFT for minimum/maximum.

NOTE: If hold last value is selected for hard fault, output 1 and output 2 must still be selected for minimum or maximum. The selection determines the state of outputs at module power-up (green LED flashing) until the load/enter sequence is complete, or power-down of +5V dc. See Table 2.C.

Table 2.B
Programming Plug Selections: Digital (left-hand) Board

Location	Function	Position
E1	Factory Configured	OUT
E2 **[1]**	Hard fault response: Hold last value Minimum/maximum value	 RIGHT LEFT
E3 through E9	Factory Configured	See figure 22
E10	Source of +5V dc Backplane External supply	 IN OUT
[1] The selection for E2 affects both outputs the same. The choice of minimum value or maximum value for the hard fault output must be made on the analog board regardless of the choice of E2. (see text and analog board plugs E4 and/or E5).		

Table 2.C
Programming Plug Selections: Analog (right-hand) Board

Choose and record the required conditions for each function below.

Function	Condition
Output 1: Hard Fault or Loss of +5V dc	Minimum Value Maximum Value
Output 2: Hard Fault or Loss of +5V dc	Minimum Value Maximum Value
Analog Input 1	Voltage Current
Analog Output 1	Voltage Current
Tieback Input 1	Voltage Current
Analog Input 2	Voltage Current
Analog Output 2	Voltage Current
Tieback Input 2	Voltage Current
Compliance	Standard (500 ohms: COMMON @ OV) Additional (1250 ohms: COMMON @ - 15V)
Source of +5V dc	Backplane External Supply

Table 2.D
Programming Plug Positions: Analog (right-hand) Board

Mark the programming plug position for each function below.

Location	Function	Position
E1	Output 2, current mode Output 2, voltage mode	LEFT RIGHT
E2	Output 2, current mode Output 2, voltage mode	LEFT RIGHT
E3	Output 1, current mode Output 1, voltage mode	LEFT RIGHT
E4	Hard fault* output 2, minimum Hard fault* output 2, maximum	IN OUT
E5	Hard fault* output 1, to minimum Hard fault* output 1, to maximum	IN OUT
E6	Output 1, voltage mode Output 1, current mode	TOP BOTTOM
E7	Output 2, voltage mode Output 2, current mode	TOP BOTTOM
E8	Output 1, voltage mode Output 2, current mode	TOP BOTTOM
E9	Factory configured	RIGHT
E11	Tieback 1, current mode Tieback 1, voltage mode	IN OUT 1
E12	Tieback 2, current mode Tieback 2, voltage mode	IN OUT 1
E13	Factory configured	LEFT
E14	Input 2, current mode Input 2, voltage mode	IN OUT 1
E15	Input 1, current mode Input 1, voltage mode	IN OUT 1
E16,17	Factory configured	BOTH IN
E18 **[2]**	Additional compliance (-15V dc) Standard compliance (OV dc)	LEFT RIGHT
E19, 20	Factory configured	BOTH IN
E21 **[2]**	Additional compliance Standard compliance	OUT 1 IN
E22**[2]**	Additional compliance Standard compliance	OUT [1] IN

Location	Function	Position
E23 **[3]**	+5V dc from backplane +5V dc from external source	TOP BOTTOM
E24 **[3]**	+5V dc from backplane +5V dc from external source	TOP BOTTOM

*or loss of +5V dc

[1] IN refers to connecting the two pins together. OUT refers to storing the programming plug by placing it over a single pin, electrically floating.

[2]The positions of programming plugs E18, E21 and E22 must be the same.

[3] The positions of programming plugs E23 and E24 must be the same.

NOTE: Use figure 2.3 to locate the programming plugs.

2. Select source of +5V dc as the backplane or external supply. Record your selection on Table 2.B by circling IN for backplane or OUT for external.

Part B)
Select and record the analog board features on Table 2.C using the following procedure.

Select the modules' response to a hard fault or loss of +5V dc. Choose maximum or minimum value for either output 1 or 2. Make these selections regardless of how you set E2 in Table 2.B. If you selected hold last value, you still must select maximum or minimum value for each output. Outputs go to the selected value at module power-up (green LED flashing) until the load/enter sequence is complete, or when powering down +5V dc.

1. Choose minimum or maximum response of output 1 for hard fault or power-down of +5V dc.

2. Choose minimum or maximum response of output 2 for hard fault or power-down of +5V dc.

3. Choose analog input 1 as either voltage mode (+1 to 5V dc) or current mode (+4 to +20mA).

4. Choose analog output 1 as voltage or current.

5. Choose the tieback input 1 as voltage or current.

If tieback input 1 is wired to track the manual control station associated with analog output 1, then both tieback input 1 and analog output 1 must be selected to the same mode of either current or voltage.

6. Choose analog input 2 as voltage or current.

7. Choose analog output 2 as voltage or current.

8. Choose tieback input 2 as voltage or current.

If tieback input 2 is wired to track the manual control station associated with analog output 2, then both tieback input 2 and analog output 2 must be selected to the same mode of current or voltage.

9. Choose compliance as standard or additional.

Compliance is defined as the maximum allowable load impedance in the current mode. The standard compliance for the PID module is 500 ohms. Additional compliance can be established for one or two loops, only if analog outputs 1 and 2 and tieback inputs 1 and 2 are all selected for the current mode.

(The condition on tieback inputs is required only when they are tracking outputs.) Additional compliance allows a maximum load impedance of 1250 ohms. Additional compliance is obtained by internally referencing the MODULE COMMON terminal to the -15V dc terminal. Choose standard or additional compliance and record in Table 2.C. The choice may affect the power supply requirement for input devices as described in section titled External Connections.

10. Choose the source of +5V dc as either the backplane or external supply.

11. Review all the choices made in table 2.C before continuing.

Part C)

Record the required programming plug positions on table 2.D using your selections on table 2.C for reference. Select LEFT/RIGHT, IN/OUT or TOP/BOTTOM so that Table 2.D has a position defined for every E location.

1. Using your selections inTable 2.C for reference, mark the corresponding plug positions in the right-hand column of Table 2.D Table 2.D. For example, if the required condition for output is minimum value due to hard fault or loss of +5V dc, mark the IN position in Table 2.D for E5.

Part D)

Set programming plugs E2 and E10 on the digital board using Table 2.B and the following procedure:

1. Remove the unmarked left cover plate to gain access to the digital circuit board.

2. Refer to Figure 2.2 to identify the location of the user-selectable and factory configured programming plugs.

3. Set programming plugs E2 and E10 according to the functions circled in Table 2.B.

4. Verify that the factory configured programming plugs are installed as shown in Figure 2.2

5. Set the completed digital board, cover, and screws to one side.

Part E)

Set the programming plugs on the analog board usingTable 2.D and the following procedure:

1. Remove the right cover (with the terminal identification label) to gain access to the analog circuit board.

2. Refer to Figure 2.3 to identify the locations of the user-selectable and factory configured programming plugs.

3. Starting at E1, read down table 2.D and set each programming plug on the analog board.

CAUTION: The programming plugs at location E11 and E12 could interfere with the front cover flange when the analog board is re-assembled to the rest of the module. This could happen when either the E11 or E12 programming plug is placed in the OUT (floating) position. When either is required to be in the OUT position, place the floating side of the E11 plug toward the center of the board and the floating side of the E12 plug toward the top of the board.

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4. Verify that factory configured programming plugs are in their correct positions.

5. Re-assemble the PID module. Typically it is easier to re-assemble the digital board and cover before the analog board and cover. Observe caution when re-assembling the analog circuit board. Be certain that the three stake pins located on the lower corner of the board mate with their respective sockets on the digital board. Carefully align these connections before aligning and tightening the screws on the module cover.

Record the I/O range selections on the module's write-on label.

Figure 2.2
Programming Plug Locations (Digital Board)

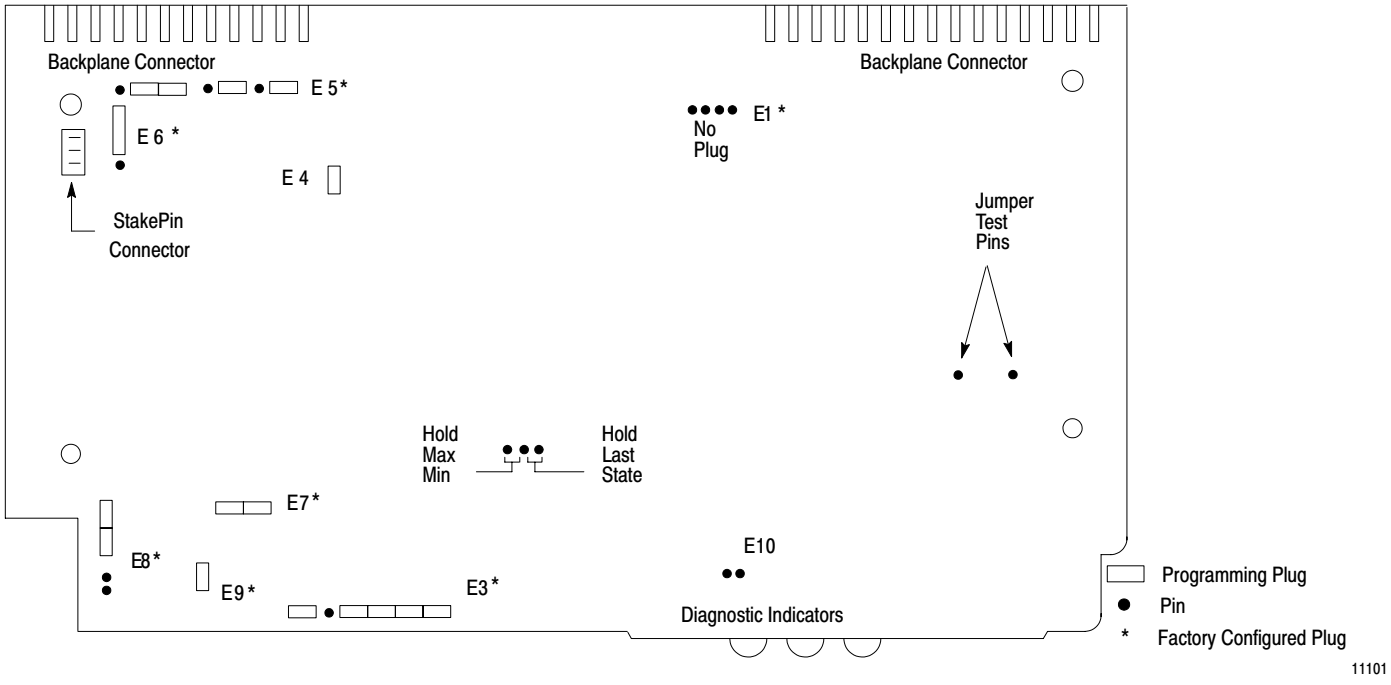
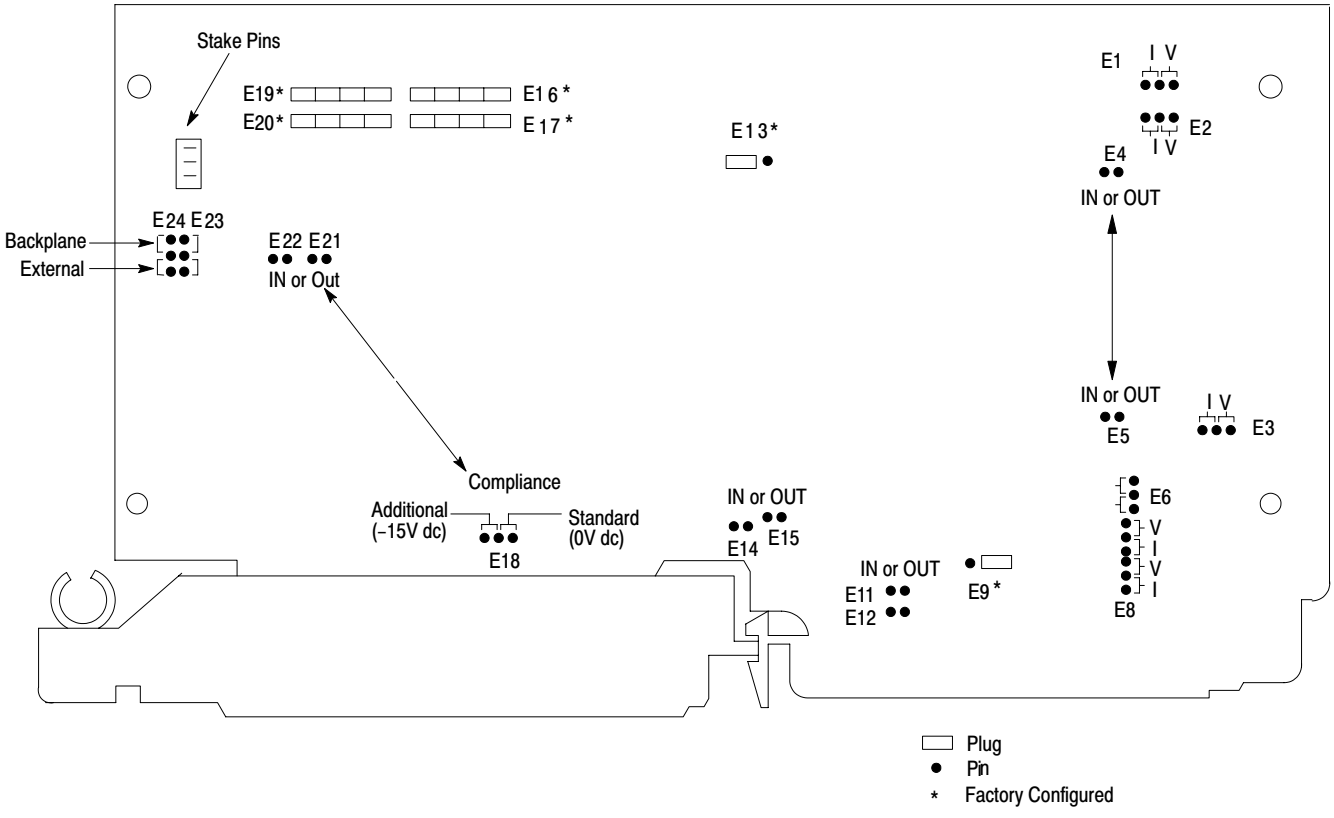


Figure 2.3
Programming Plug Locations (Analog Board)



External Connections

Terminal identification of the PID module's field wiring arm and general connections are shown in Figure 2.4. Typical I/O connections for a single closed loop configured in current mode are shown in Figure 2.5. The remaining three figures show typical connections to input and output devices and control mode connections to a manual control station.

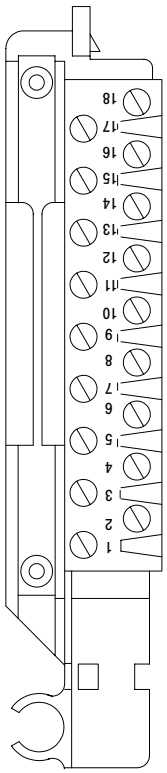
Figure 2.6 shows typical connections to input devices without a manual control station. When an input loop is configured in current mode, the input impedance of all devices connected in series must be considered when selecting the input power supply. the input loop could contain one or more recording devices (250 ohms) and/or a manual control station (100 ohms) in addition to the PID module (250 ohms) and the current transmitter. Current transmitters typically require at least 18V dc. Voltage transmitters, if used, draw their power from a supply independent of the input circuit.

Figure 2.7 shows typical connections to actuators when the output is monitored by the tieback input. Note that when a tieback input is not used to monitor a voltage output, the jumper to the TIEBACK INPUT terminal is not connected. When the tieback input is not used to monitor a current output, the return from the actuator is connected to MODULE COMMON, not to the TIEBACK INPUT terminal. The module monitors tieback inputs only when you enable manual mode of the manual control station described below.

Figure 2.8 shows the connections from the PID module to a manual control station required for switching control automatically to the station or manually at the station. The wiring is the same for PID module outputs configured in current or voltage mode.

The MANUAL REQUEST terminal permits the PID module, upon detecting a hard fault or when under PC processor control, to switch the manual control station from automatic to manual mode. The MANUAL MODE terminal is used to inform the PID module when the station is in manual mode. The TIEBACK INPUT terminal monitors the station output and allows a bumpless transfer of control from the manual control station to the PID module.

Figure 2.4
Terminal Identification and Connections



Terminal Identification
Cat. No. 1771-PDC

Terminal	Function	
18	Input 1 (+ Lead)	Process Variable 1
17	Input 1 (– Lead)	
16	Input 2 (+ Lead)	Process Variable 2
15	Input 2 (– Lead)	
14	Tieback Input 1	Tieback Input 1 [1]
13	Tieback Input 2	Tieback Input 2 [1]
12	Analog Output 1	Control Element 1
11	Module Common [2]	Module Common
10	Analog Output 2	Control Element 2
9	+15V DC	Required +15V DC Power Supply (cat. no. 1770-P1, 1778-P2, or equivalent)
8	± 15V DC Common	
7	–15V DC	
6	Manual Mode 1	[3]
5	Manual Mode 2	[3]
4	Manual Request	[4]
3	OPT. +5V DC Common	Optional +5V DC Power Supply [5] (cat. no. 1771-P2 or equivalent)
2	Optional +5V DC	
1	Not Used	

[1] The tieback inputs can be used to track manual control station output to provide bumpless transfer, or can be used as feedforward inputs.

[2] Module common signal level can be selected to either ±15V DC COMMON (system common) for standard compliance, or –15V DC for additional compliance depending on the application.

[3] When the manual control station is in manual, the station switches these line to the MODULE COMMON terminal.

[4] When a request for manual is made from the PID module or when this relay contact output is used for alarm annunciation, the line is switched to the module common signal level for 50 msec. For hardware failure or loss of analog power (±15V DC), this relay output is held at module common until the fault is corrected.

[5] Programming plugs must be positioned for optional +5V DC supply.

11097

Figure 2.5
Typical Connections for 1-Loop Control

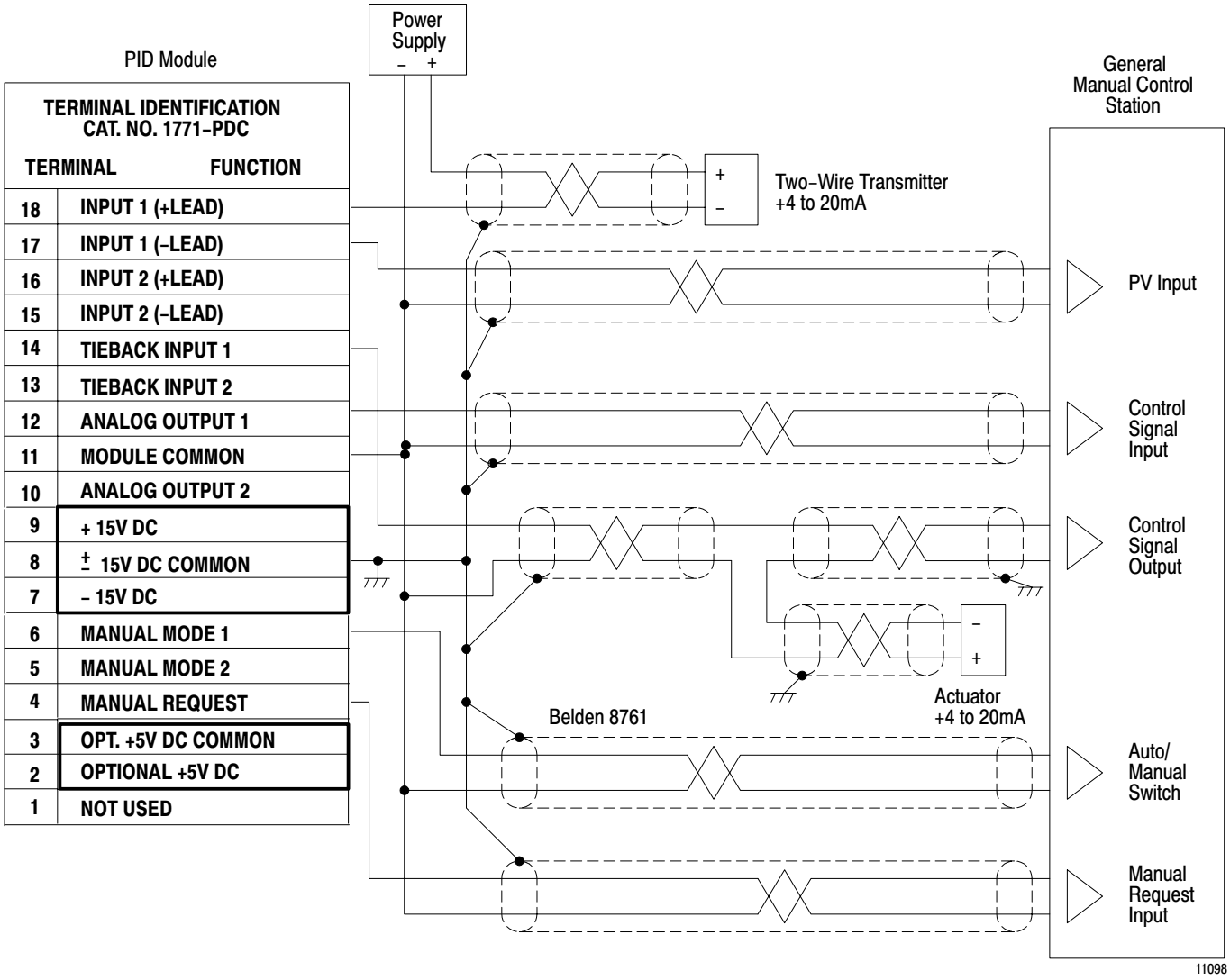


Figure 2.6
Connections to Input Devices

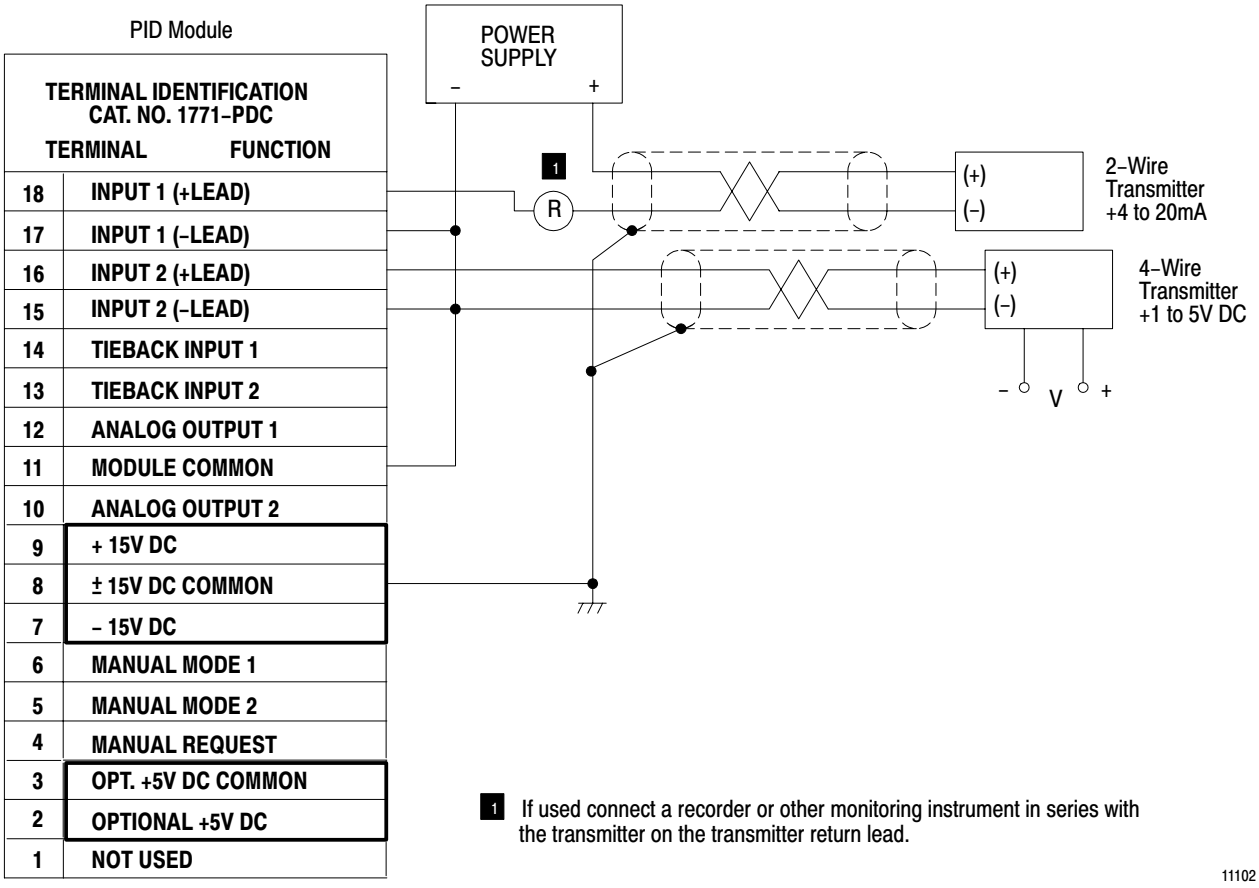
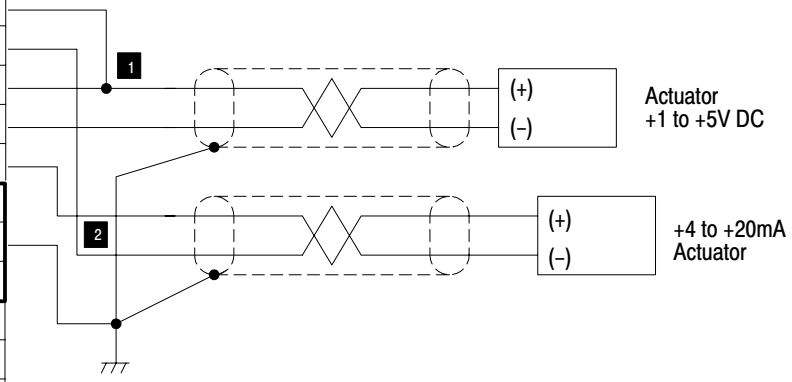


Figure 2.7
Connections to Output Actuators

PID Module

TERMINAL IDENTIFICATION CAT. NO. 1771–PDC	
TERMINAL	**FUNCTION**
18	INPUT 1 (+LEAD)
17	INPUT 1 (–LEAD)
16	INPUT 2 (+LEAD)
15	INPUT 2 (–LEAD)
14	TIEBACK INPUT 1
13	TIEBACK INPUT 2
12	ANALOG OUTPUT 1
11	MODULE COMMON
10	ANALOG OUTPUT 2
9	+ 15V DC
8	± 15V DC COMMON
7	– 15V DC
6	MANUAL MODE 1
5	MANUAL MODE 2
4	MANUAL REQUEST
3	OPT. +5V DC COMMON
2	OPTIONAL +5V DC
1	NOT USED

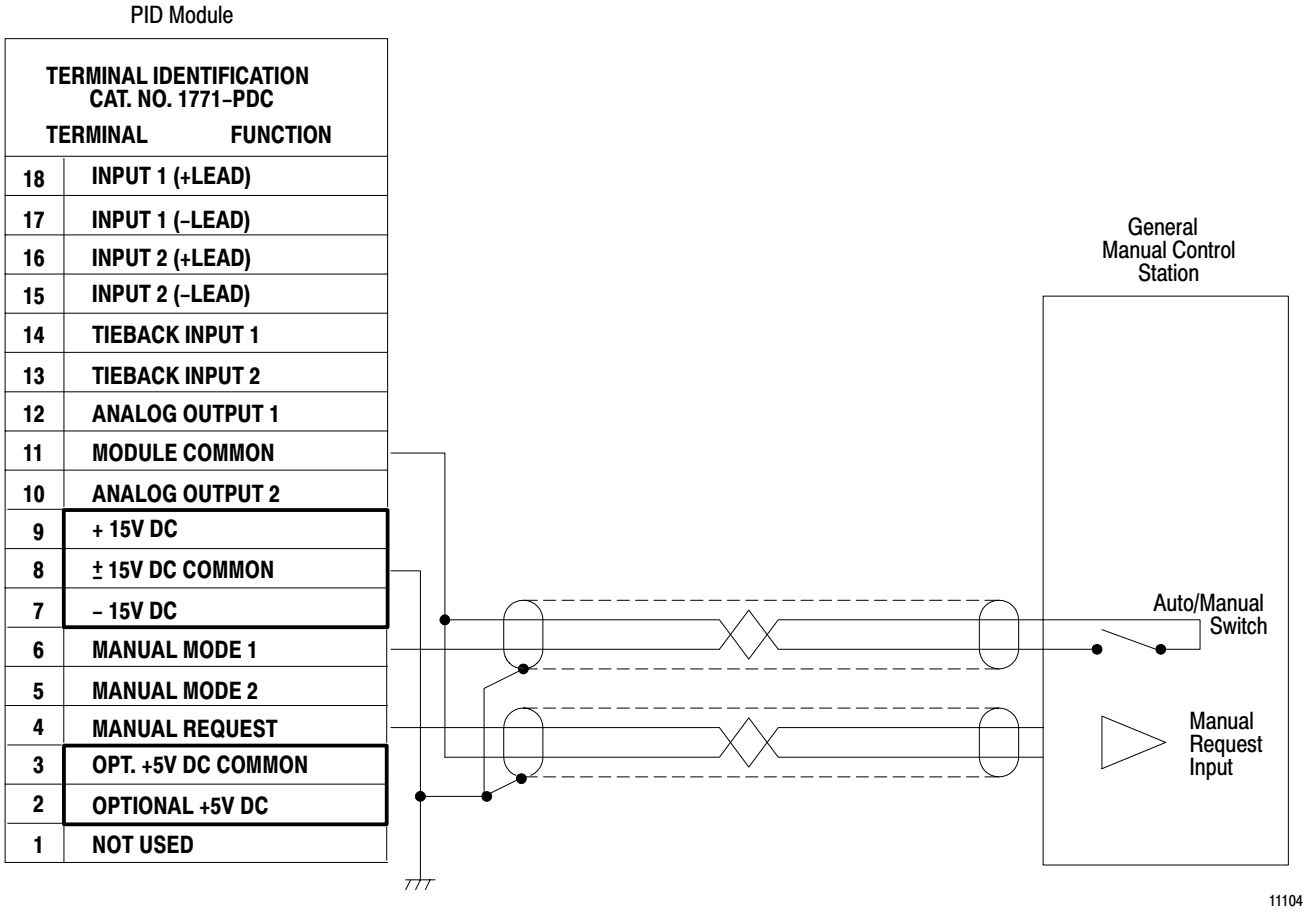


1 If tieback is not used to monitor a voltage output, do not make this connection.

2 if tieback is not used to monitor a current output, connect the return lead to MODULE COMMON terminal 11.

11103

Figure 2.8
Control Mode Connections to Manual Control Station



Manual Control Station Interface

The PID module is designed for use with commercially available manual control stations, one per loop. The station is connected between the analog output and the controlled element of the process. The station provides manual override control and automatic backup to the PID module. Manual control stations can be used for start-ups, on-line process adjustments, and routine maintenance. The station can be used in either of two ways, manual override control or module back-up.

Manual Override Control

An operator can override automatic control by switching to manual control and adjusting the output at the manual control station. When the manual control station is switched to manual mode, a connection is closed between the MANUAL MODE terminal (referenced to +15V dc) and the MODULE COMMON terminal on the PID module (Figure 2.8). This

allows the PID output to be switched open at the manual control station and a manually controlled output to be switched into the system.

When in manual mode, care should be taken not to return to automatic control when the output is below +1V dc or +4mA. If attempted, an output surge could occur. The PID module performs a bumpless transfer when the tieback input is tracking a signal at or above the minimum level of +1V dc or +4mA. Also, the PID module's operating mode must include integral control and the manual mode status line must be closed at the manual control station. The module monitors tieback inputs only when you enable manual control.

Module Back-up

The manual control station can be used to automatically backup the PID module in the event of module failure. A module failure would de-energize the PID module's contact output and generate a manual request to the manual control station causing control to be transferred in the following manner.

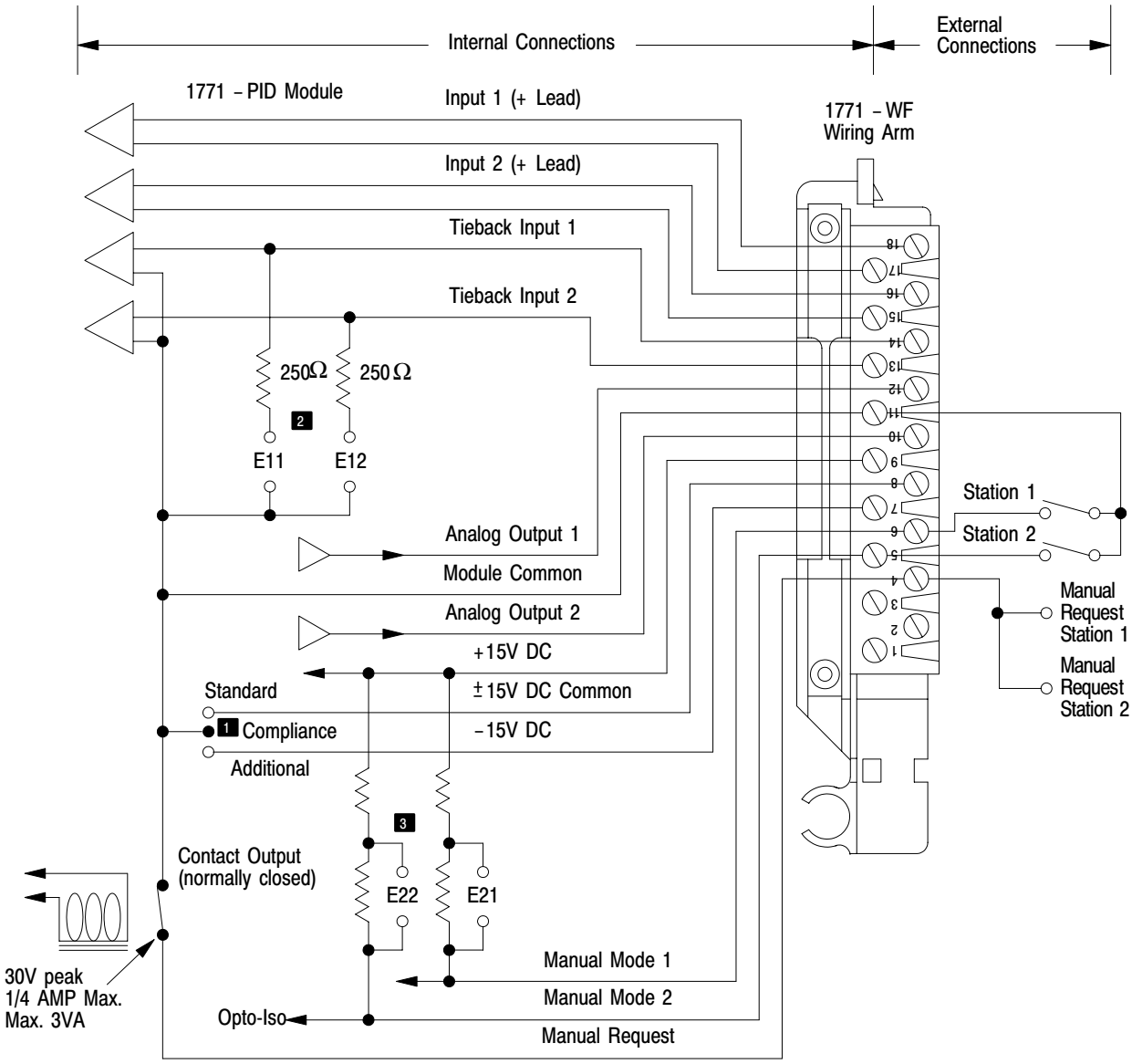
The contact output (Figure 2.9) is a normally closed contact. When the PID module is in normal operation, the contact will be held open. A manual request is generated by contact closure. The contact will close and remain closed in the event of module failure or loss of $\pm$15V dc analog power. Contact closure internally switches the signal at terminal 4 MANUAL REQUEST to terminal 11 MODULE COMMON. There is only one contact output. If two manual control stations are used, both will be switched simultaneously.

If a manual request is generated by program logic, contact closure is a one-shot 50 millesecond closure. The closure can be used to activate an alarm device by connecting a latching relay to terminal 4 MANUAL REQUEST and terminal 11 MODULE COMMON on the PID module.

Once the PID module relinquishes control to the manual control station, the plant operator must physically reset the operation to automatic mode using a switch on the manual control station.

When control is returned from manual to automatic at the manual control station, the PID module performs a bumpless transfer if the tieback analog input is used to track the output from the manual control station and the PID module's operating mode includes integral control.

Figure 2.9
Internal Connections to the Field Wiring Arm



NOTE: Optional +5V DC power supply wiring is not shown.

1 Standard compliance selects module common as ±15V DC Common (500Ω max for current outputs)
Additional compliance selects module common as –15V DC Common (1250Ω max for current outputs.)

2 Programming plugs inserted for current mode.

3 Programming plugs inserted for standard compliance.

11105

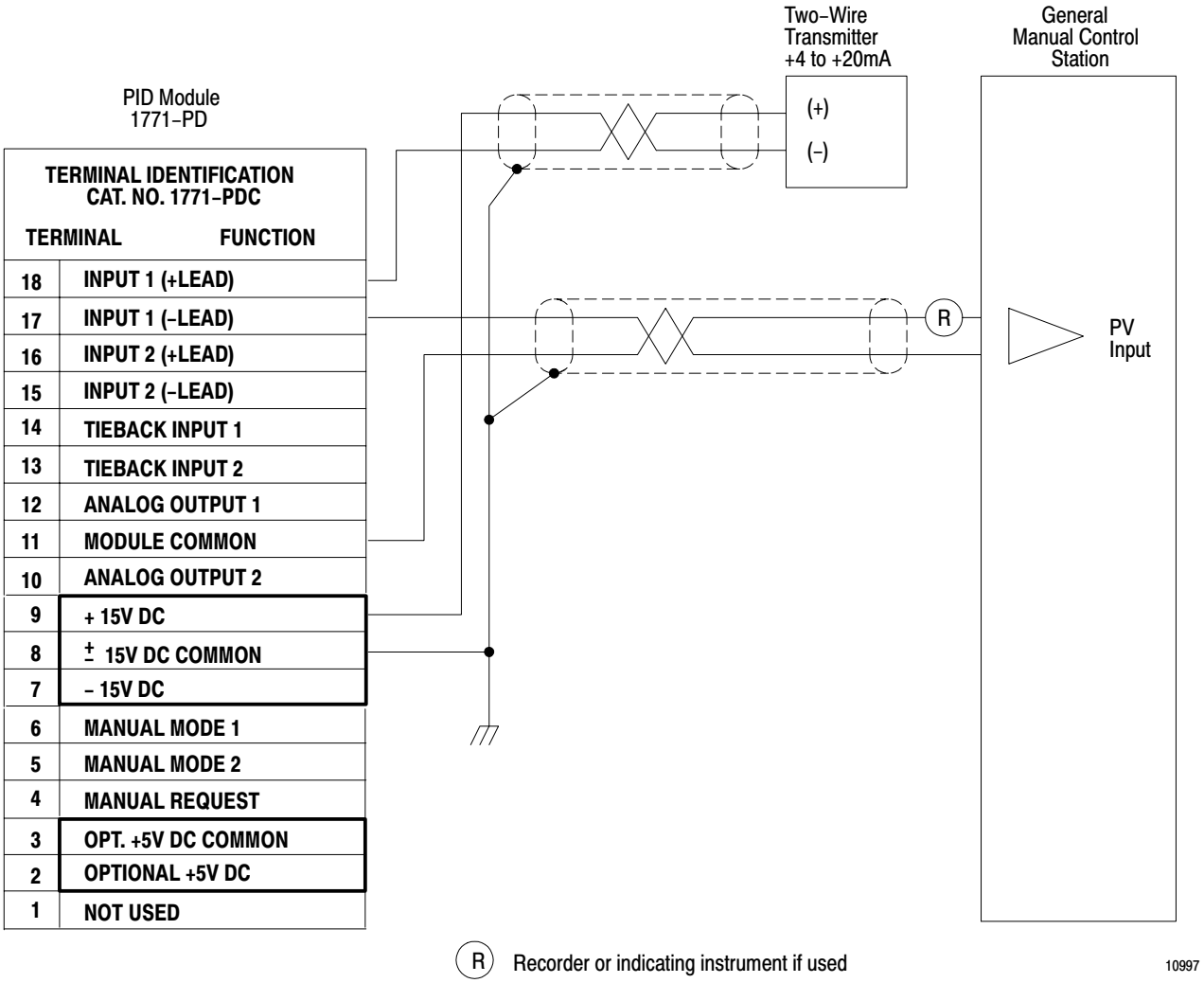
Input Power Supply Requirements

The source of power for the input loop when the input is configured for current mode can be either the analog ±15V dc supply or a separate supply. The choice depends on the selected output compliance and the number of devices in the loop.

±15V dc Analog Supply

When both the module outputs and tieback inputs (if used) are configured in current mode, additional compliance can be selected. As such, module common is internally connected to -15V dc. The ±15V dc analog power supply can provide a 30 V dc source to the input current loop by jumpering the +15V Dc terminal of the PID module to the positive lead of the current transmitter (Figure 2.10). The potential of 30 V dc is enough to provide the required voltage drops for the transmitter, PID module, and manual control station.

Figure 2.10
Current Mode Input Using External ±15V dc Supply



Separate Supply

If additional compliance is not selected (as when one of the module outputs is configured in voltage mode), a separate DC power supply must be used to power the input current loop.

Power Supply Voltage

When selecting the power supply to operate the input current loop, the required voltage must be equal to the voltage drop across all impedances at the maximum current of 20mA. Current transmitters typically require a voltage drop of 18V dc or more. The process variable input impedance of the PID module (250 ohms), manual control station (100 ohms), recording

or indicating instrument if used (typically 250 ohms) must be considered when calculating the voltage drop in the loop.

For example, the required voltage for an input loop that contained the PID module, manual control station, and current transmitter that requires at least 18V dc would be 18V +2 (250 ohms) (.020 amps)= 18V +10V = 28V dc. Up to 2 V dc could be allowed for voltage drops in the cables when using a 30 V dc source such as the ±15V dc analog power supply with the module output configured for current operation and additional compliance.

If the input loop were to contain a chart recorder and an indicating instrument (250 ohms each) in addition to the basic loop in the previous example, the power supply would have to provide a least 38V dc plus an amount equal to the voltage drop of the cables. A separate power supply would have to be used.

Power Supply Current

The ±15V dc analog power supply must provide 100mA to the PID module's analog circuits. This includes 20mA that the module provides to each output current loop. If the ±15V dc supply is providing 20mA to each input current loop, a 2-loop control system will require 140mA. This is within the specification for the Allen-Bradley 1770-P1 power supply rated at 150mA at ±15V dc.

Installation Practices

To minimize the effects of electromagnetic interference (EMI), group analog modules together in the I/O chassis whenever possible. Avoid placing PID modules close to AC modules or high voltage DC modules.

It is important to use shielded cable when wiring analog signals. Belden 8761 or equivalent cable has an insulated twisted pair of conductors covered by a foil shield. To reduce the effect of EMI induced noise along the cable, the shield must be properly grounded at one end, only. The recommended grounding point for each cable is identified in the wiring diagram (Figure 2.5-Figure 2.8 and Figure 2.10). One end of the shield should be cut short and taped to insulate it from any electrical contact. The other end should be tied to a common point at earth ground.

Optional Instrument Grounding Bus

An alternate grounding system can be used to separate analog signal ground from the grounding of equipment such as motor starters and are

welders which generate high electrical noise. Equipment grounding can carry electrical noise when ground loops exists.

The alternate grounding method is for instruments, only. A instrument ground bus is located inside the enclosure containing the I/O chassis, manual control station, and PC processor. The instrument bus is electrically isolated from the I/O chassis and enclosure. The bus is connected to earth ground by a direct path, independent of other equipment ground connections.

When using instrument grounding, the only change to the connection drawings (Figure 2.5 through Figure 2.8 and Figure 2.10) is that the chassis ground symbol would be redefined as instrument ground. All cable shields and the ±15V dc COMMON terminal of the PID module would be connected to the instrument ground bus.

When multiple PID modules are placed in the same chassis, the ±15V dc commons and +5V dc commons, if used, should be connected to the ground bus at one point. Do not daisy-chain the commons.

Chassis Considerations

The PID dual-slot module must be placed with single module group when placed in a I/O chassis. Up to eight PID modules can be placed in a single 128 I/O chassis. Up to four of the PID modules can be powered from the +5V I/O chassis power supply. The remaining PID modules, if installed, must be powered by a separate +5V dc supply through the field wiring arm +5V dc and 5V dc COMMON terminals. Be sure that the total current requirement for all modules in the I/O chassis using the I/Ochassis power supply does not exceed the rating of the I/O chassis and the I/O chassis power supply.

Avoid placing the PID module close to AC I/O modules or high voltage DC I/O modules. It cannot be inserted in the left-most slot reserved for the processor module in a single I/O chassis system or for the I/O adapter module in a multi-chassis system.

Set switch 1 of the I/O chassis last state switch assembly to the off position to allow PID module operation in soft fault mode. Refer to section titled Loop Control Word B for additional information on soft fault mode selection.

Other intelligent I/O modules can operate without interference in the same I/O chassis with PID modules.

Internal Fusing

The PID module has internal pico fuses to protect circuitry from surges in the optional +5V dc supply., A blown fuse condition is indicated when none of the front panel LED indicators turn on after you turn on this supply. If the LEDs do not turn on, check programming plugs E23 and E24. These plugs allow you to select the source of +5V dc from the backplane or from an external supply. Incorrect positioning of these plugs can prevent the LEDs from turning on even when pico fuses are OK. Check that E23 and E24 are in the correct position for using the external +5V dc supply (Table 2.D and Figure 2.3).

If the fuses are blown, we recommend that you return the module for factory repair through your nearest field service or sales office. Unauthorized repair of these fuses could result in damage to other circuit components and void your warrantee.

Precautions

Take the following precautions to avoid blowing these fuses:

- Be sure that the optional +5V dc supply is connected correctly to field wiring arm terminals (Figure 2.4).
- Be sure that the optional +5V dc supply meets specifications (Table 2.G), especially for surge voltage at turn on.
- Supply +5V dc to each PID module using one or more optional external power supplies.
- Place an on/off switch in the +5V dc lead to each PID module. This allows you to remove power and replace a PID module without turning off power to other PID modules in the chassis.
- Remove power from the PID Module's field wiring arm before connecting or disconnecting the arm.

Recommendations for Installing or Removing Modules

We make the following recommendations for removing one of several PID modules from an I/O chassis.

WARNING: Remove power from a field wiring arm before connecting or disconnecting it. Turn off power to the I/O chassis before inserting or removing any of its modules. Failure to observe this warning can result in damage to module circuitry and/or unpredictable operation of other modules in the chassis with possible damage to equipment and/or injury to personnel.

- Place PID modules in one or more chassis containing only PID modules.
- Supply +5V dc to each PIC module using one or more optional external power supplies.
- Place an on/off switch in the +5V dc lead to each PID module. This allows you to remove power and replace a PID module without turning off power to other PID modules in the chassis.

Removal of a Faulted PID Module

You can replace a faulted PID module in an I/O chassis using the following procedure if each PID module is supplied with +5V dc from a separate power supply or from a common supply with a switch in each +5V dc lead.

1. Select the soft fault mode that allows PID modules to continue operation when they lose communication with the PC processor. Do this by means of your ladder program.

2. Turn off power to the I/O chassis. Block transfers cease but PID modules continue to operate.

3. Turn off the +5V and ±15V dc power to the faulted module.

4. Replace the faulted PID module.

5. Turn on power to the module and I/O chassis.

6. Restore the original soft fault mode to the PID modules.

If there are other modules and/or other PID modules without an external +5V dc supply, they cease to operate when you turn off power to the chassis. After restoring power, you must download PID control parameters to PID modules through a load/enter sequence.

PID modules (rev C or later) have the option for you to select how outputs respond when +5V dc is removed from the module. You select either maximum or minimum, output using programming plus (refer to titled Programming Plug Selection).

Keying

The backplane connector should be keyed to accept only this module after its position in the I/O chassis has been determined.

Plastic keying bands shipped with the I/O chassis should be used. The position of the keying bands on the upper backplane connector must correspond to the mating slots on the module connector.

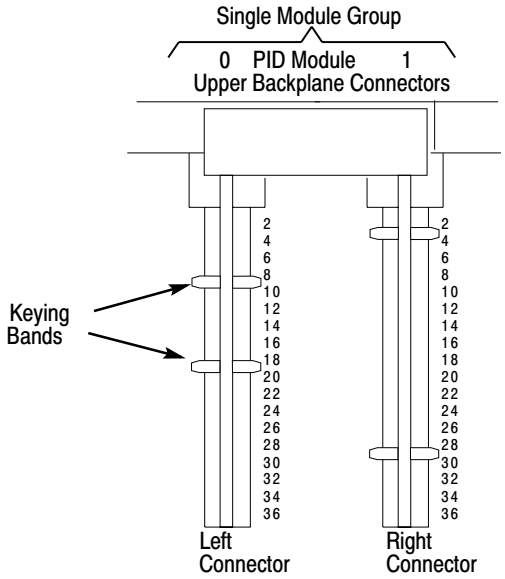
Refer to Figure 2.11. Using needle-nose pliers, place the keying bands on the backplane connector between these numbers:

Slot 0 (left)
8 and 10
18 and 20

slot 1 (right)
2 and 4
28 and 30

The position of the keying bands can be changed if subsequent system design requires the module to be moved to a different location.

Figure 2.11
Keying Diagram



Power Supply Specifications

Isolation must be maintained between the analog and digital circuits of the PID module to minimize electrical noise interference. Therefore, separate power supplies must be used for the analog ±15V dc supply and for the digital +5V dc supply.

The requirements for the customer ±15V dc power supply and for the optional +5V dc power supply are listed in Table 2.E and Table 2.F, respectively.

Table 2.E
Customer ± 15V dc Power Supply Requirements

Specifications	+15 Volts	-15 Volts
Output Current	100mA	100mA
Output Voltage Tolerance	1%	1%
Regulation (type)	Series	Series
Line Regulation (for 10V AC input change)	±0.2%	±0.2%
Load Regulation (no load to full load)	±1.0%	±1.0%
Ripple	10mVpp	10mVpp
Overvoltage Protection **[1]**	+18V dc	-18V dc
Current Limit (percent of full load)	125%	125%
[1] The module is not protected from overvoltages from the customer power supply.		

Table 2.F
+5V dc Power Supply (Optional) Requirements

Specifications	+5Volts
Voltage (at wiring arm)	5.05V dc
Current	1.2A per PID module
Voltage Regulation	Sum of all deviations due to line, load, and ripple should not exceed ±0.15V dc
Rise Time (to 4.75V dc)	Less than 10msec

Module Specifications

The PID module specifications are listed in Table 2.G.

Table 2.G
Specifications

Process Variable Inputs	**Digital Resolution**	**Maximum Current**
Number	12-binary, 1 part in 4095	250mA
process variable input 1	**Accuracy**	**Maximum Power**
process variable input 2	±0.1% of range at 25^0C	3VA
Configuration	**Input Impedance**	**Digital Inputs (from manual**
Differential	250 ohms (current)	**manual control station)**
Range (user-selectable)	4.7 megohms (voltage)	Two independent inputs for moni-
+4 to +20mA	**Maximum Allowable Input**	toring
+1 to +5V dc	±30mA (current)	**Power Requirements**
Digital Resolution	25V rms (voltage)	**Backplane or External (Digital Circuits)**
12-bit binary, 1 part in 4095	**Temperature Coefficient**	1.2A at +5V dc
Accuracy	±50 ppm/^{0}C	**External (Analog Circuits)**
±0.1% of range at 25^0C	**Analog Outputs**	100mA AT +15V dc
Input Impedance	**Number**	100mA at -15V dc
250 ohms (current)	analog output 1	**Loop Update Time**
10 megohms (voltage)	analog output 2	100msec, typical
Common Mode Rejection Ratio	**Configuration**	**Ambient Temperature Ratings**
70dB DC	Single ended	Operation 0^0C to 60^0C (32^0F to
Common Mode Voltage Range	**Range (user-selectable)**	140^0F
±200V with respect to module	+4 to +20mA	Storage -40^0C to 85^0C (-40^0F to
common	(With output common internally	185^0F)
Common Mode Input Resistance	referenced to power supply	**Relative Humidity Rating**
2.5 megohms	common	5% to 95% (without condensation)
Input Frequency Respnse	the output will drive up to a 500 ohm	**Electrical Isolation**
-3dB at 1kHz	load over the full current range.[1]	1500V rms (transient
Maximum Allowable Input	+1 to +5V dc	(Isolation is achieved by
±30mA (current)	(500 ohms minimum load resistance	optoelectronic coupling between I/O

125V dc (voltage)

Temperature Coeffeicient

±50 ppm/^{0}C

Tieback Inputs

Number

tieback input 1

tieback input 2

Configuration

Single ended

Range (user-selectable)

+4 to +20mA

+1 to +5V dc

10mA maximum load current.)

Digital Resolution

12-bit binary, 1 part in 4095

Accuracy

±0.1% of range at 25^{0}C

Temperature Coefficient

±50 ppm/^{0}C

Contact Output

Number

one normally closed contact,held open

Peak Voltage

30V

analog circuit and control logic)

Keying

Left connector (slot 0) between 8 and 10, 18 and 20

Right connector (slot 1) between 2 and 4, 28 and 30

[1] If all analog outputs and tieback inputs used are selected to current mode, the compliance of the analog outpus can be extended from 500ohms (standard compliance to 1250 ohms(additional compliance). This is achieved by internally referencing the outputs to -15V dc.

Chapter 3

Programming

General

Before starting to program the PID module, read this entire chapter thoroughly. Be sure that the programming plug functions have been selected as described in section titled Programming Plug Selection.

The PID module can be programmed in four general steps:

1. Choose the PID module features required for the application. These are listed in section titled Capabilities (chapter 1) and are presented in the algorithm flow chart (Figure 3.15).

2. Identify the control bits and loop storage words which must be programmed to implement the features. These are defined in section titled Word and Bit Definitions. Record the values of the storage words and the logic state of the control bits on the worksheets found in appendix A.

3. Write the ladder diagram program and assign data table addresses to the data blocks used to store loop values. The examples presented in appendix B or C should be used as guides.

4. Using a industrial terminal, enter the program into memory and the block data into the data table. Refer to the worksheets on which the values of the loop storage words have been recorded. Set the appropriate control bits.

Sections listed below provide information for selecting PID module features and programming the module.

- Section titled Operational Overview provides an overview of the programming concepts which are used to program and monitor the PID module.
- Section titled Word and Bit Definitions defines the words and bits which can be used to program the module.
- Section titled Algorithm Flow Chart contains the algorithm flow chart and explains it use.
- Section titled Block Transfer Programming explains how the module is programmed using block transfer instructions.

- Section titled Programming Consideration explains the application of block transfer instructions.
- Section titled Expanded Features describes the expanded features of the PID module and how they can be applied.

Additionally, four appendices contain helpful programming information:

- Appendix A contains the worksheets which are used to record data that is entered into the PC processor and transferred to the PID module.
- Appendix B describes a program that performs continuous block transfers to the PID module. This program may be used when continuous parameter adjustment or continuous reporting of module status is required for a critical application.
- Appendix C describes a program that performs periodic block transfers to the PID module. This program may be used when less frequent parameter adjustment is required.
- Appendix D contains summary word and bit tables and a word/bit reference.

Operational Overview

The PID module is a closed loop process controller with proportional, integral, and derivative control action. Control algorithm features are user determined and loaded in the PID module by block transfer from the PC processor. The PID module is equipped to control up to two process control loops using its internal microprocessor. Because the features of the two loops are similar, the description will be general to both loops except where otherwise stated. Each loop is individually configured with its own parameter values.

PID Algorithm

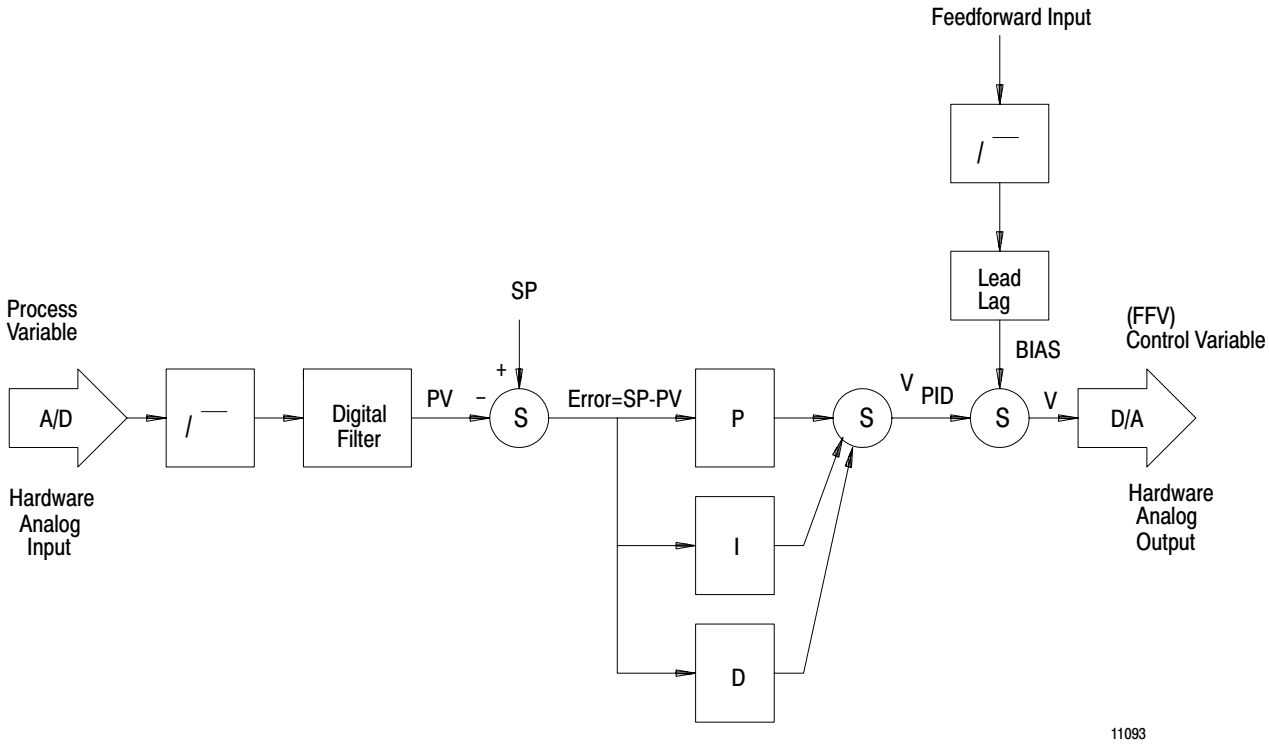
The PID module contains features which are user-selected to perform the desired control. Figure 3.1 is a simplified diagram of the PID module features. Basically, the PID module reads the process variable, compares it to the set point, and adjusts the analog output to make the process variable equal the set point. The process variable PV is the analog input from the process. The setpoint SP is the equilibrium value of the process, and the analog output is the control variable to the process. The difference between the set point and the process variable is the error signal, E=SP-PV.

The PID module can perform a combination of proportional, integral and derivative control. Integral control is also known as reset action. Derivative control is also known as rate action. The PID module can perform relatively simple or very complex control based on selected

features. The full algorithm flow chart is presented in section titled Algorithm Flow Chart.

The PID module (rev C or later) uses the ISA algorithm (P, I and D dependent gains) or the Allen-Bradley algorithm (P, I and D independent gains). Refer to appendix E for algorithm comparison and selection. Earlier revision modules use only the Allen-Bradley algorithm.

Figure 3.1
Simplified PID Algorithm



Block Transfer Data Blocks

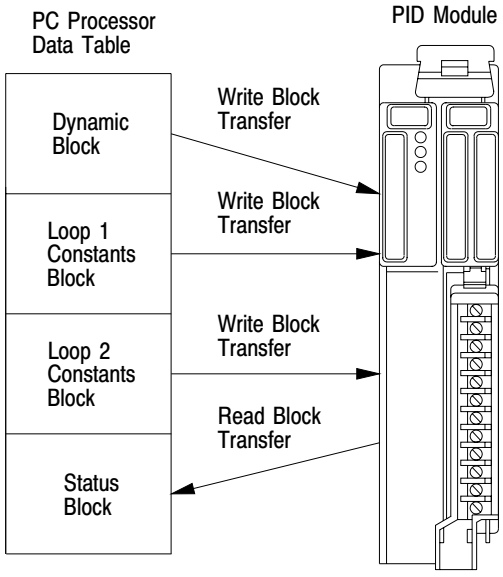
Data block files are areas of the PC processor data table used to store loop control words and loop values. The features of the module are selected by setting word and bit values in data block files. The data block files are transferred to the PID module by block transfer instructions.

Three write block transfers are required to load the PID module with data from three data table block files. The dynamic block DB contains values which are subject to change for both loops. The loop 1 block LP1 and loop 2 block LP2 contain loop constants which seldom change.

The status block SB is a read block transfer file used to report the current status of the PID module and any alarm condition detected by the module. The transfer of the status block is also used to prompt the next write block transfer.

Figure 3.2 illustrates the multiple block concept.

Figure 3.2
Multiple Block Concept

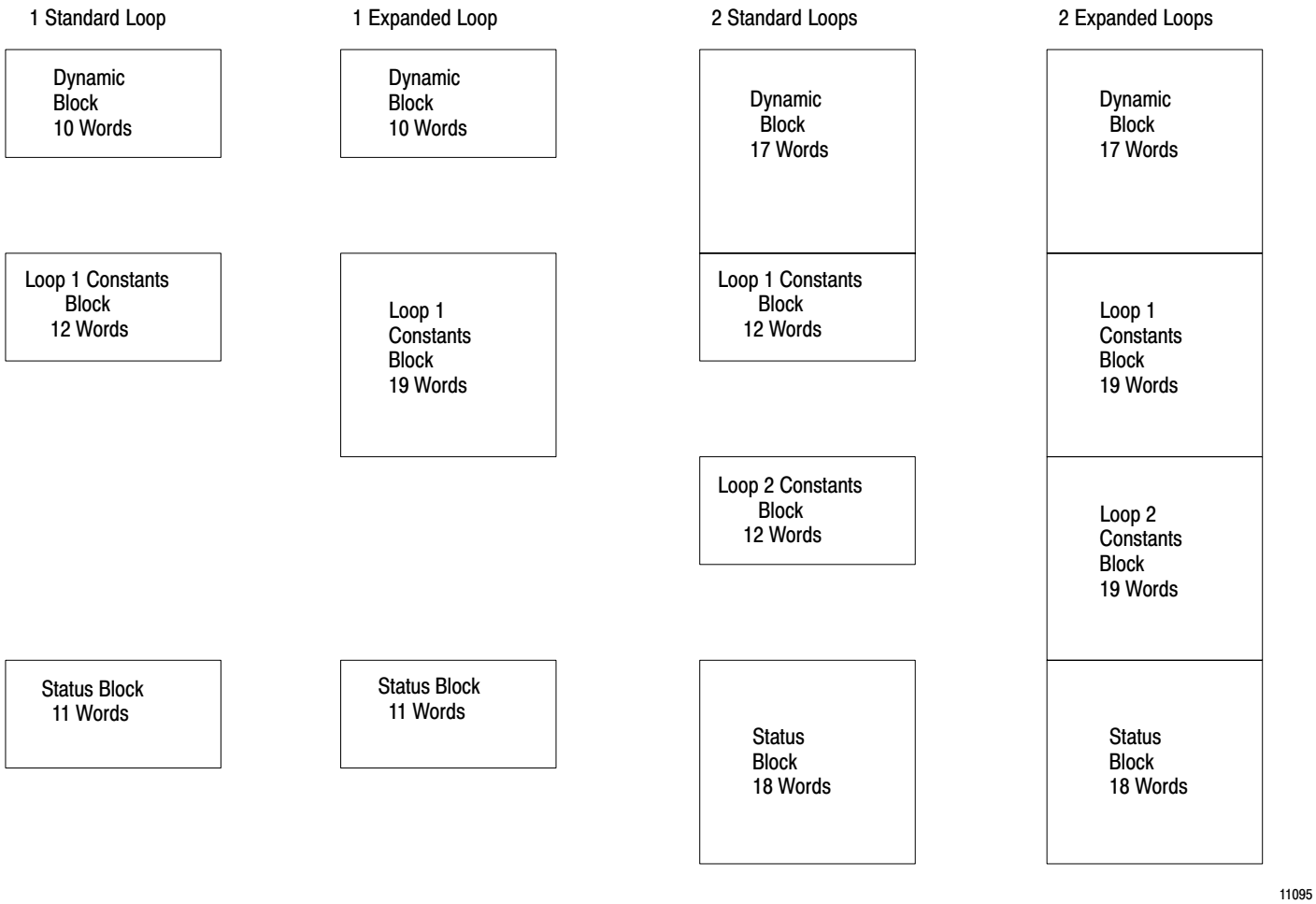


PC Processor Memory Requirements

The PID module requires multiple files in the C processor data table to store the different blocks of data. Storage requirements are determined by the features selected. The module can be configured for one or two loops with either standard or expanded features. There are four different memory requirements for storing block of data (Figure 3.3).

User program memory requirements will vary depending on the application. Examples are shown in appendicies B and C.

Figure 3.3
Block File Memory Requirements



Load/Enter Sequence

The load/enter sequence is used when all PID control parameters (dynamic block and loop block data) are transferred from the PC processor to the PID module. The load/enter sequence is required at power-up and whenever it is necessary to change any of the loop constants in LP1 or LP2 or selected control bits in the master control word. (After a load/enter sequence has been completed, dynamic block data can be changed at any time by a write block transfer). Changes to loop constants require a load/enter sequence as a safety consideration to prevent inadvertent changes which could adversely affect the system.

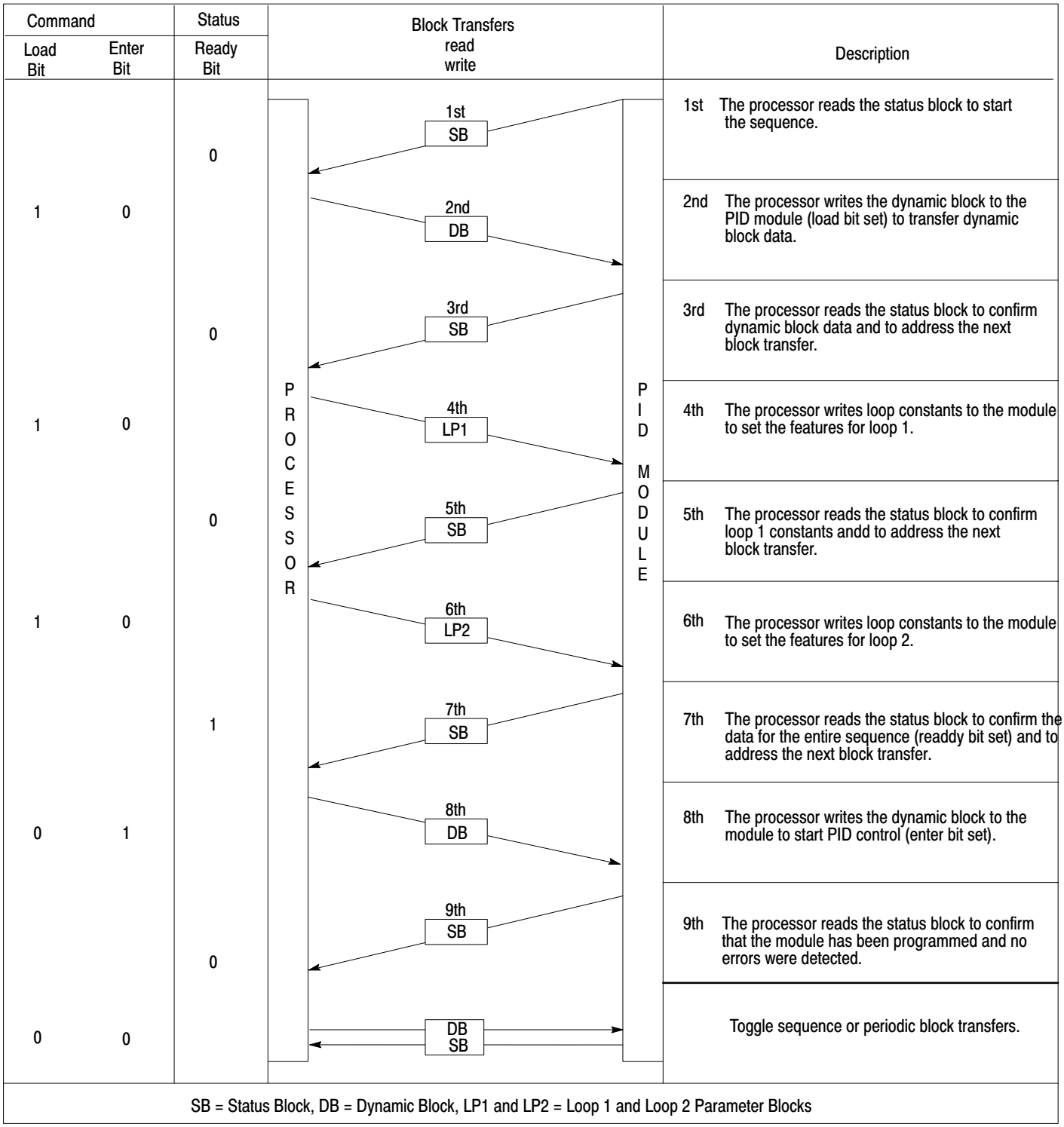
The PID module prompts the sequencing of block transfers. The write block transfer instruction in the user program contains the data table address of the first word of the block file to be transferred. By manipulating this address, different data block files can be transferred with the same write block transfer instruction.

There are three control bits which are associated with the handshaking of the load/enter sequence.

- The load bit is set in the dynamic block to allow the PID module to accept dynamic block data and to load loop 1 and loop 2 constants into the module's buffer.
- The ready bit is returned in the status block to indicate that the write block transfers were acceptable and that the module is able to process the information.
- The enter bit is set to activate the information in the module's buffer and to start control based on the new parameters transferred during the load/enter sequence.

An overview of the load/enter sequence is presented in Figure 3.4. Additional information can be found in sections titled Power-up Load/Enter Sequence and Load/Enter Sequence.

Figure 3.4
Load/Enter Sequence



11107

Word and Bit Definitions

This section defines the words and bits of the three write blocks and the single read block. For ease of reference, the following word and bit notation is used throughout the manual:

A PID module word is abbreviated as Wxx.
Example: Word number 12 = W12.

A PID module bit is abbreviated as Bxx.
Example: Bit number 07 = B07.

The word and bit abbreviations can be used together.
Example: Word number 12, Bit number 07 = W12 B07.

Other notations which will be used are (LE) and (XF). The symbol (LE) is used to designate the four bits in the master control word which require a load/enter sequence to occur before the PID module will accept a change to them. The symbol (XF) is used to designate words or bits which are used to select the Expanded Features of a loop.

For ease of reference, the parameter words required to program the module are numbered consecutively in the following sections.

Section titled Dynamic Block: Words W01-W17.

Section titled Loop Constants Block: W18-W36 for loop 1, W38-W56 for loop 2.

Section titled Status Block: W57-W74.

Dynamic Block: Words W01-W17

The dynamic block is a write block transfer file of up to 17 words. It is used to establish the features of the PID module, to program the most frequently changing (dynamic) parameters of loop 1 and loop 2, and to load information required by the PID module for controlling the block transfer sequences.

If loop 1 is selected, only words W01 must be programmed. If both loops are selected, then the entire 17 word block must be programmed.

The 17 words of the dynamic block are defined in the paragraphs that follow. Table 3.A lists the dynamic block words. All the words of the

dynamic block, loop blocks and status block are listed in Table 3.J, Figure 3.13 and Figure 3.14 found at the end of section title Word and Bit Definitions.

Table 3.A
Dynamic Block Words

Word	Title	Abbreviation
W01	Master Control Word	
W02	Control Word	
W03	Dynamic Block Start Address	
W04	Loop 1 Block Start Address	
W05	Set Analog Output 1	SET OUT 1
W06	Set Point 1	SP1
W07	Proportional Gain 1	K_p1
W08	Bias 1	BIAS 1
W09	**Set Process Variable 1**	SET PV1
W10	**Set Feedforward Input 1**	SET FFI1
W11	Loop 2 Block Start Address	
W12	Set Analog Output 2	SET OUT 2
W13	Set Point 2	SP2
W14	Proportional Gain 2	K_p2
W15	Bias 2	BIAS 2
W16	**Set Process Variable 2**	SET PV2
W17	**Set Feedforward Input 2**	SET FFI2

W01 Master Control Word. This word initiates all activities in the PID module from power-up. This word programs the module configuration, controls the initiation of the block transfer sequences, and can control the setting of the analog outputs and the contact output. Bits 17 through 00 are defined below and summarized in Figure 3.5.

W01 B17, B16 Block Identifiers. Both bits must be set to 1 to identify this block as the dynamic block.

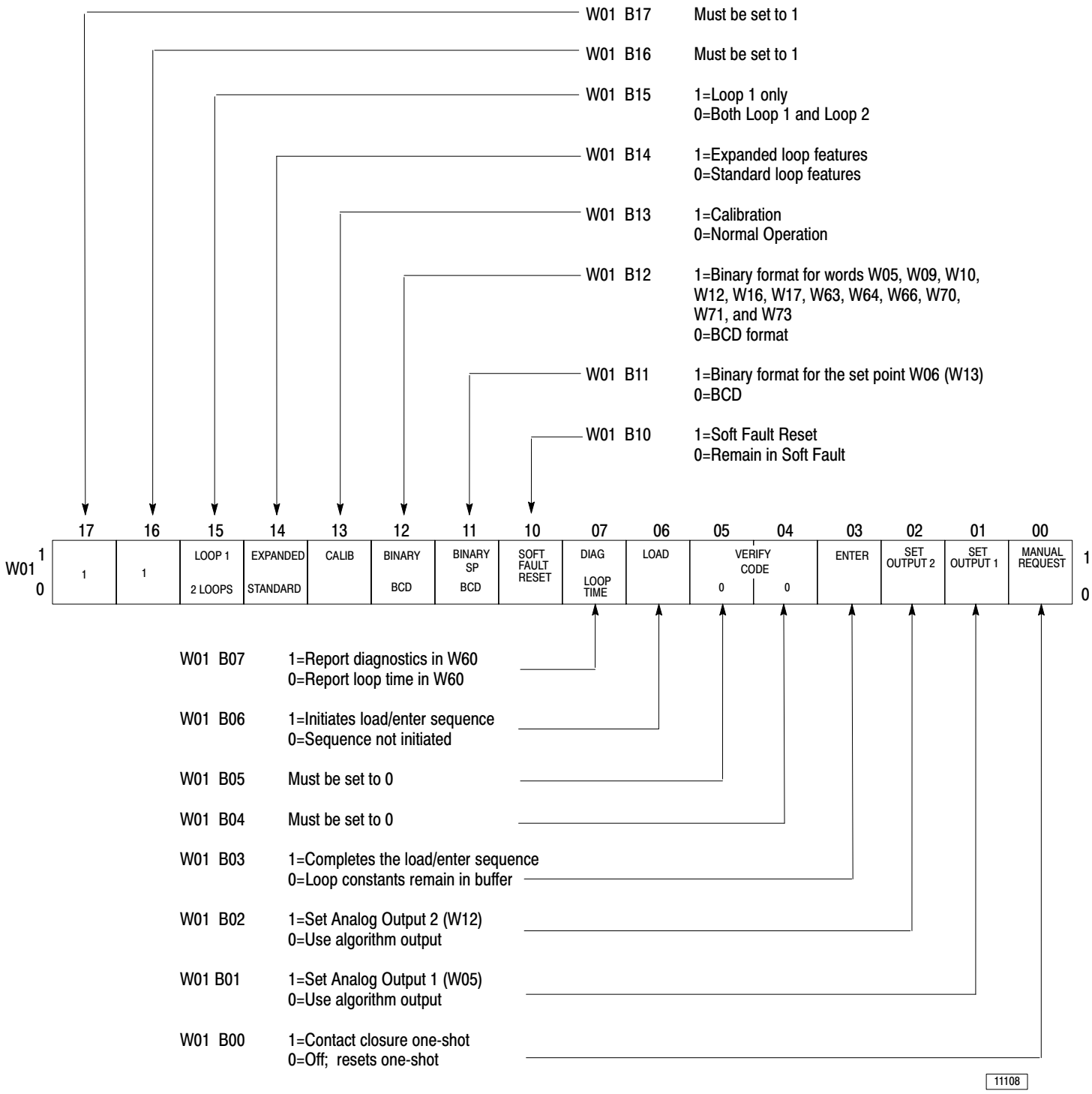
W01 B15 Loop Select. **[LE]** Reset to 0 selects both loop 1 and loop 2. Set to 1 selects loop 1 only. When loop 1 and loop 2 are selected, all words in the dynamic block are used and both loop blocks must be programmed. When loop 1 is selected, only words W01 through W10 of the dynamic block are used and the loop 1 block must be programmed.

W01 B14 Standard/Expanded Features. **[XF], [LE]** Reset to 0 selects standard loop features. When the stand loop is selected, loop 1 words W30 through W36 and loop 2 words W50 through W56 are NOT used by the module. Set to 1 selects expanded loop features

such as feedforward, scaling, lead/lag, and all the words in the loop block must have a value. The value of unused expanded feature words must be zero.

W01 B13 Calibration. Reset to 0 selects normal operation. Set to 1 only for calibrating the module. This bit is examined only at power-up, and is used with W02 B17 and B16.

Figure 3.5
Master Control Word W01



W01 B12 Binary/BCD Format. [LE] Reset to 0 selects the 4-digit BCD (4095 maximum) format. Set to 1 selects the 12-bit are listed in Table 3.B.

Table 3.B
Binary/BCD Format Words

Word	Title	Word	Title
W05	Set Analog Output 1	W63	Read Loop 1 Output
W09	Set Process Variable 1	W64	Read Analog Input 1
W10	Set Feedforward Input 1	W66	Read Tieback Input 1
W12	Set Analog Output 2	W70	Read Loop 2 Output
W16	Set Process Variable 2	W71	Read Analog Input 2
W17	Set Feedforward Input 2	W73	Read Tieback Input 2

W01 B11 Set Point Format. [LE] Reset to 0 selects 4-digit BCD (4095 maximum) format for set point 1 in word W06 and set point 2 in word W13. Set to 1 selects the 12-bit binary (4095 maximum) format. If scaling has been selected by B16 = 1 in word W30 for loop 1 or in W50 for loop 2, the 4-digit BCD value has the data format of 9999.

W01 B10 Soft Fault Reset. Reset to zero holds the module in soft fault mode until this bit is set to 1. Set to 1 allows recovery from the soft fault mode after the fault is corrected. Soft fault mode is signified by W58 B10 = 1 and is indicated by the flashing STAND-ALONE yellow LED on the PID module. The soft fault mode of operation is selected by bits B15, B14, B13 in word W19 for loop 1 and W39 for loop 2.

W01 B07 Loop Time/Diagnostic. Reset to 0, causes word W60 to report loop update time. Set to 1 causes word W60 to report error codes. The upper byte of word W 60 reports dynamic block error codes. The lower byte reports error codes and loop 1 and loop 2 blocks.

W01 B06 Load. Reset to 0 inhibits the load/enter sequence. Set to 1 initiates the load/enter sequence.

When the load bit is set, the loop constants are loaded into the module's buffer. They are not used until the enter bit is set at the completion of a load/enter sequence. The same applies to the four bits in the master control word W01 B15, B14, B12, B11 designed

by (LE). These bits are protected from accidental change because they control the number of PID loops, standard or expanded loop features and binary or BCD data format. These bits can be changed in the same manner that loop constants are changed, only by a load/enter sequence. The remaining bits in the master control word and the remaining dynamic block words can be changed at any time by a write block transfer. See sections titled Power-Up Load/Enter Sequence and Load/Enter Sequences.

W01 B05, B04 Verify. Both bits must be set to 0 for normal operation.

W01 B03 Enter. Used with load bit W01 B06 to complete a load/enter sequence. when 0, the data previously loaded remains in the module's buffer. Set to 1 the buffered data is moved from the buffer into the module's active area and the sequence is completed. The buffered data includes all loop constants and the four (LE) bits in the master control word W01 B15, B14, B12, B11. See sections titled Power-Up Load/Enter Sequence and Load/Enter Sequence.

W01 B02 Set Output 2. Reset to 0 selects the analog output value determined by the module's PID algorithm. Set to 1 selects the analog output as the value stored in word W12, Set OUT2, downloaded from the PC processor. When reset to 0, the analog output value is adjusted automatically from the SET Out value to the value determined by the PID algorithm, a bumpless transfer.

W01 B01 Set Output 1. Reset to 0 selects the analog output value as determined by the module's PID algorithm. Set to 1 selects the analog output as the value stored in word W05, SET OUT1, downloaded from the PC processor. When reset to 0, the analog output value is adjusted automatically from the SET OUT value to the value determined by the PID algorithm, a bumpless transfer.

W01 B00 Set Manual Request. Reset to 0 the PID module inhibits contact closure. Set to 1 generates a contact closure for 50msec. To repeat this one-shot closure, it is necessary to first reset this bit to 0 and then set it to 1 again.

W02 Control Word. Use this word to select ISA or A-B values for the PID algorithm, or to select module calibration.

W02 B17, B16 Calibration. Refer to chapter 5.

W02 B00 PID Algorithm. Reset to 0 the PID module uses A-B gain values. Set to 1 the PID module uses ISA values.

W03 Dynamic Block Start Address. This word contains the data table address of the first word in the file associated with the dynamic block. The address is required by the PID module to prompt the transfer of the dynamic block.

W04 Loop 1 Block Start Address. This word contains the data table address of the first word in the file associated with the loop 1 block. The address is required by the PID module to prompt the transfer of loop 1 constants.

W05 Set analog Output 1, SET OUT1. The value stored in this word becomes the analog output when W01 B01 = 1.

Normally, the PID module outputs the PID algorithm value when W01 B-1 = 0. Data format is 4-digit BCD or 12-bit binary. Format is determined by W01 B12. Range is 0000 to 4095.

W06 Set Point 1, SP1. This word contains the set point value for loop 1. Data format is 4-digit BCD or 12 bit binary as selected by W01 B11. The unscaled range is 0000 to 4095.

When set point scaling is selected, the data format should be 4-digit BCD. Scaling can be selected by B16=1 in word W30 when expanded loop features are selected by W01 B14 = 1. The sign bit W19 B07 and the x10 multiplier bit W19 B06 determine the range which can be $\pm$99990.

When scaling is selected, words W31 and W32 must contain the minimum and maximum range values SMIN1 and SMAX1, respectively. Refer to section titled Scaling for additional information about scaling.

W07 Proportional Gain 1, Kp1 (Kc1). This word contains the proportional gain constant for loop 1. The value is the same for A-B (Kp1) or ISA (Kc1), selected by W02 B00. Data format is 4 digit BCD (99.99 dimensionless) with implied decimal point. Multiplier bit W19 B04, B05 can be selected for x1, divided by 10, x10, x100 (Table 3.F, Multiplier Codes). By using multipliers, the range can be extended from 0.000 to 9999.

W08 Bias 1, BIAS1. When using only standard loop features, the loop bias is the value stored in this word. When expanded loop features are selected by W01 B14 = 1, either the feedforward term FFV or the value stored in this word can be used as the loop bias. The feedforward term is normally used unless W30 B02 = 1 which sets the bias to the value stored in this word.

The data format is 4-digit BCD, range 0000 to 9999. When expanded loop features are selected, the negative bias bit W30 B01 = 1 allows a full-scale range of ±9999.

W09 Set Process Variable 1, SET PV1. The value stored in this word is used by the PID module as the process variable for loop 1 when W18 B15 =1. Normally, the PID module uses the hardware analog input value when W18 B15 = 0. Data format is 4-digit BCD or 12-bit binary. Format is selected by W01 B12. Range is 0000 to 4095.

W10 Set Feedforward Input 1, SET FFI1. (XF) The value stored in this word is used by the PID module as the feedforward input when W30 B13 = 0. The PID module uses the tieback input 1 value as the feedforward input when W30 B13 = 1. This word can be used only when expanded loop features are selected by W01 B14 = 1. Data format is 4-digit BCD or 12-bit binary. Format is selected by W01 B12. The range is 0000 to 4095.

NOTE: The following words are programmed if the module is configured for 2-loop operation, W01 B15 = 0.

W11 Loop 2 Block Start Address. This word contains the data table address of the first word in the file associated with the loop 2 block. The address is required by the PID module to prompt the transfer of the loop 2 constants.

W12 Set Analog Output 2, SET OUT2. The value stored in this word becomes the analog output when W01 B02 = 1. Normally, the PID module outputs the PID algorithm value when W01 B02 = 0. Data format is 4-digit BCD or 12-bit binary. Format is selected by W01 B12. Range is 0000 to 4095.

W13 Set Point 2, SP2. This word contains the set point value for loop 2. Data format is 4-digit BCD or 12-bit binary as selected by W01 B11. The unscaled range is 0000 to 4095.

When set point scaling is selected, the data format should be 4-digit BCD. Scaling can be selected by B16 = 1 in word W50 when expanded loop features are selected by W01 B14 = 1. The sign bit W39 B07 and the x10 multiplier bit W19 B06 determine the range which can be ±99990.

When scaling is selected, words W51 and W52 must contain the minimum and maximum range values SMIN2 and SMAX2, respectively. Refer to section 3.6.1 for additional information about scaling.

W14 Proportional Gain 2, Kp2 (Kc2). This word contains the proportional gain constant for loop 2. The value is the same for A-B (Kp2) or ISA (Kc2), selected by W02 B00. Data format is 4-digit BCD (99.99 dimensionless) with implied decimal point. Multiplier bits W19 B04, B05 can be selected for X1, divided by 10, x10, x100 (Table 3.F, Multiplier Codes). By using multipliers, the range can be extended from 0.000 to 9999.

W15 Bias 2, BIAS2. When using only standard loop features, the loop bias is the value stored in this word. when expanded loop features are selected by W01 B14 = 1, either the feedforward term FFV or the value stored is this word can be used as the loop bias. The feedforward term is normally used unless W50 B02 = 1 which sets the bias to the value stored in this word.

The data format is 4-digit BCD, range 0000 to 9999. When the expanded loop features are selected, the negative bias bit W50 B01 = 1 allows a full scale range of ±9999.

W16 Set Process Variable 2, SET PV2. The value stored in this word is used by the PID module as the process variable for loop 2 when W38 B15 = 1. Normally, the PID module uses the hardware analog input value when W38 B15 = 0. Data format in 4 digit BCD or 12-bit binary. format is selected by W01 B12. Range is 0000 to 4095.

W17 Set Feedforward Input 2, SET FF12. (XF) The value stored in this word is used by the PID module as the feedforward input when W50 B13 = 1. Normally, the PID module uses the tieback input 2 value as the feedforward input when W50 B13 = 0. This word can be used only when expanded loop features are selected by W01 B14 = 1. Data format is 4-digit BCD or 12-bit binary. Format is selected by W01 B12. The range is 0000 to 4095.

Loop Constants Block: W18-W36 for Loop 1, W38-W56 for Loop 2

Loop block are write block transfer files of up to 19 words. They contain loop constants and are used to establish the loop features of the PID module. Loop 1 block must be used when the PID module is controlling only one loop. The loop 1 and loop 2 blocks are used for 2-loop control. Three control words are used to select the features in each loop. They are loop control words A and B, and the expanded loop control word. The remaining words are used to store values which typically remain constant during normal operation.

Loop 1 words W18 through W29 are programmed if standard features are selected by W01 B14 = 0. The entire block (words W18 through W36) is programmed if the expanded loop features are selected by W01 B14 = 1.

When both loops are used, loop 2 words W 38 through W49 must also be programmed for standard features when W01 B14 = 0. The entire loop 2 block (words W38 through W56) must also be programmed if the loop 2 expanded features are selected by W01 B14 = 1.

To change the programming of any word or bit in the loop blocks, a load/enter sequence must be initiated.

The 19 words that comprise the loop block are defined in the paragraphs that follow. Table 3.C lists the loop block words. All the words of the dynamic block, loop blocks and status block are listed in Table 3.J, Figure 3.13 and Figure 3.14 found at the end of section titled Word and Bit Description.

NOTE: Because the loop 1 and loop 2 blocks are very similar, the definitions of the words and bits will be presented once for loop 1. Reference to loop 2 will be indicated by parentheses, i.e. (loop 2).

Table 3.C
Loop Block Words

Word	Title	Abbreviation
Standard Features		
W18(W38)	Loop Control Word A	
W19 (W39)	Loop Control Word B	
W20 (W40)	Input Filter Time Constant	TA
W21 (W41)	Maximum Negative Error	EMN
W22 (W42)	Maximum Positive Error	EMP
W23 (W43)	Dead Band	DB
W24 (W44)	Integral Gain	K_I
W25 (W45)	Derivative Gain	K_D
W26 (W46)	Integral Term Limit	V_IMAX
W27 (W47)	Derivative Term Limit	V_DMAX
W28 (W48)	Minimum Output Limit	VMIN
W29 (W49)	Maximum Output Limit	VMAX
Expanded Features		
W30 (W50)	Expanded Control Word	
W31 (W51)	Minimum Scaling Value	SMIN
W32 (W52)	Maximum Scaling Value	SMAX
W33 (W53)	Feedforward Offset	FFO
W34 (W54)	Feedforward Gain	K_F
W35 (W55)	Lead Time Constant	TB
W36 (W56)	Lag Time Constant	TC

W18 (W38) Loop Control Word A. This word together with loop control word B, W19 (W39), and loop expanded control word, W30 (W50), select the configuration for the loop. Bits 17 through 00 of loop control word A are defined below and summarized in Figure 3.6 for loop 1 word W18 and loop 2 word W38.

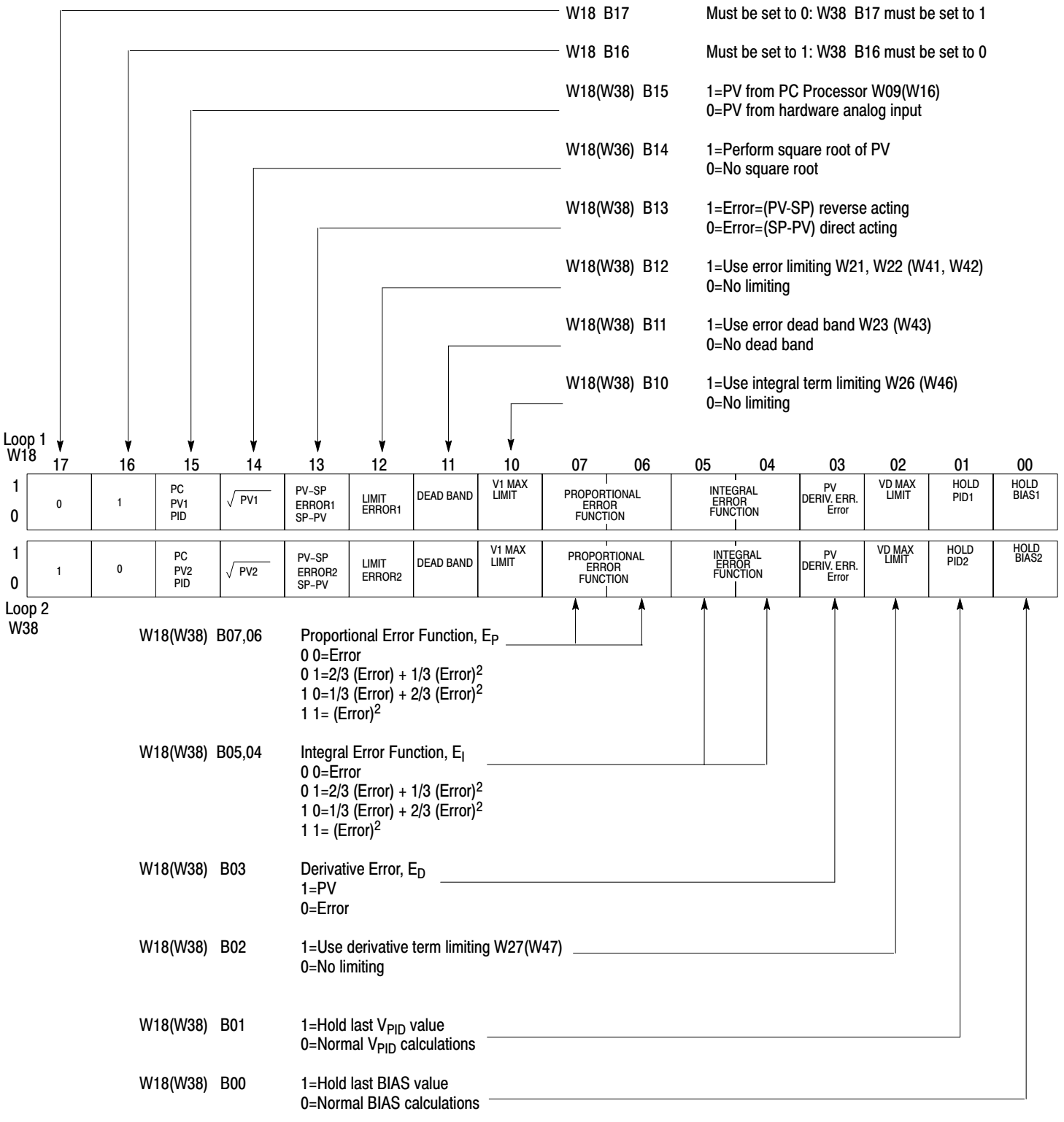
W18 (W38) B17, B16 Block Identifiers. These two bits identify this block as the loop block. B17 = 0 and B16 = 1 for loop 1. (For loop 2, B17 = 1, B16 = 0.)

W18 (W38) B15 Source of Process Variable. Reset to 0 selects the analog input as the process variable input for the loop. Set to 1 selects the value SET PV in word W09 (W16) as the process variable for the loop.

W18 (W38) B14 Square Root of Process Variable. Reset to 0 inhibits the square root function. Set to 1 enables the normalized square root of the process variable, (square root of PV x (square root of 4095). Square root allows the linearization of differential pressure type flow transducers.

(W38) B13 Error Polarity. Reset to 0 defines the error as SP-PV for direct acting control. Set to 1 defines the error as PV-SP for reverse acting control.

Figure 3.6
Control Word A, Loop 1 W18 and Loop 2 W38



Note: If you change a loop 1 or loop 2 parameter, you must initiate a load/enter sequence

W18 (W38) B12 Error Limit. Reset to 0 inhibits error limiting. Set to 1 the maximum negative error term for the loop is limited to the value EMN in word W21 (W41). The maximum positive error is limited to value EMP in word W22 (W42).

W18 (W38) B11 Dead Band. Reset to 0 inhibits dead band. Set to 1 enables the dead band feature using the value in word W23 (W43). Refer to word W23 (W43) Dead Band.

W18 (W38) B10 Maximum Integral Term Limit. Reset to 0 inhibits integral term limiting. Set to 1 the value of the integral term V_I is limited to the maximum value V_I MAX in word W26 (W46). This limit applies to both the negative and positive excursions of the integral term V I.

W18 (W38) B07, B06 Proportional Term Error. The setting of the 2-bit code determines which error signal will be used for the proportional term V_P calculation. The choices of the proportional error term E_P include straight error and error squared. Note that the sign is retained. The error codes are listed in Table 3.D.

W18 (W38) B05, B04 Integral Term Error. The setting of the 2-bit code determines which error signal will be used for the integral term V_I calculation. The choices of the integral error term E_I include straight error and error squared. Note that the sign is retained. The error codes are listed in Table 3.D.

W18 (W38) B03 Derivative Term Error. Reset to 0 the error signal is used in the derivative calculation. Set to 1 the process variable signal is used.

Table 3.D
Error Function Codes

W18(W38)			
V_P V_I	B07 B05	B06 B04	Error Function
	0 0	0 1	Error 2/3 (Error) + 1/3 $(Error)^2$
	1 1	0 1	1/3 (Error) + 2/3 $(Error)^2$ $(Error)^2$
Where $(Error)^2 = \frac{Error\|Error\|}{512}$			

W18 (W38) B02 Maximum Derivative Term Limit. Reset to 0 inhibits derivative term limiting. Set to 1 the value of the derivative term VD is limited to the maximum value VD MAX in word W27 (W47). This limit applies to both negative and positive excursions of the derivative term VD.

W18 (W38) B01 Hold PID Calculation. Reset to 0 continues the PID algorithm calculation. Set to 1 holds the PID algorithm output VPID at its last value. The hold is useful when turning the feedforward portion of the loop.

W18 (38) B00 Hold Bias. Reset to 0 continues the bias calculation. Set to 1 holds the bias at its last value. The hold is useful when tuning the PID portion of the loop.

W19 (W39) Loop Control Word B. This word together with loop control word A, W18 (W38), and the loop expanded control word, W30 (W50), select the configuration for the loop. Bits 17 through 00 are defined below and summarized in Figure 3.7 for loop 1 control word B W19, and loop 2 control word B W 39. Note that bits B11, B10, B07, and B06 are valid only if the expanded loop feature has been selected by W01 B14 = 1.

W 19 (W39) B17 VPID +/xBias. Reset to 0 the output is the sum V = VPID + BIAS. Set to the output is the normalized product V = (VPID x BIAS)/4095. The sum is normally used.

W19 (W39) B16 Output Limiting. Reset to 0 inhibits output limiting. Set to 1 the analog output value is limited to the minimum

value VMIN in word W28 (W48) and the maximum value VMAX in word W29 (W49). Limiting is not performed on the SET OUT value in word W05 (W12).

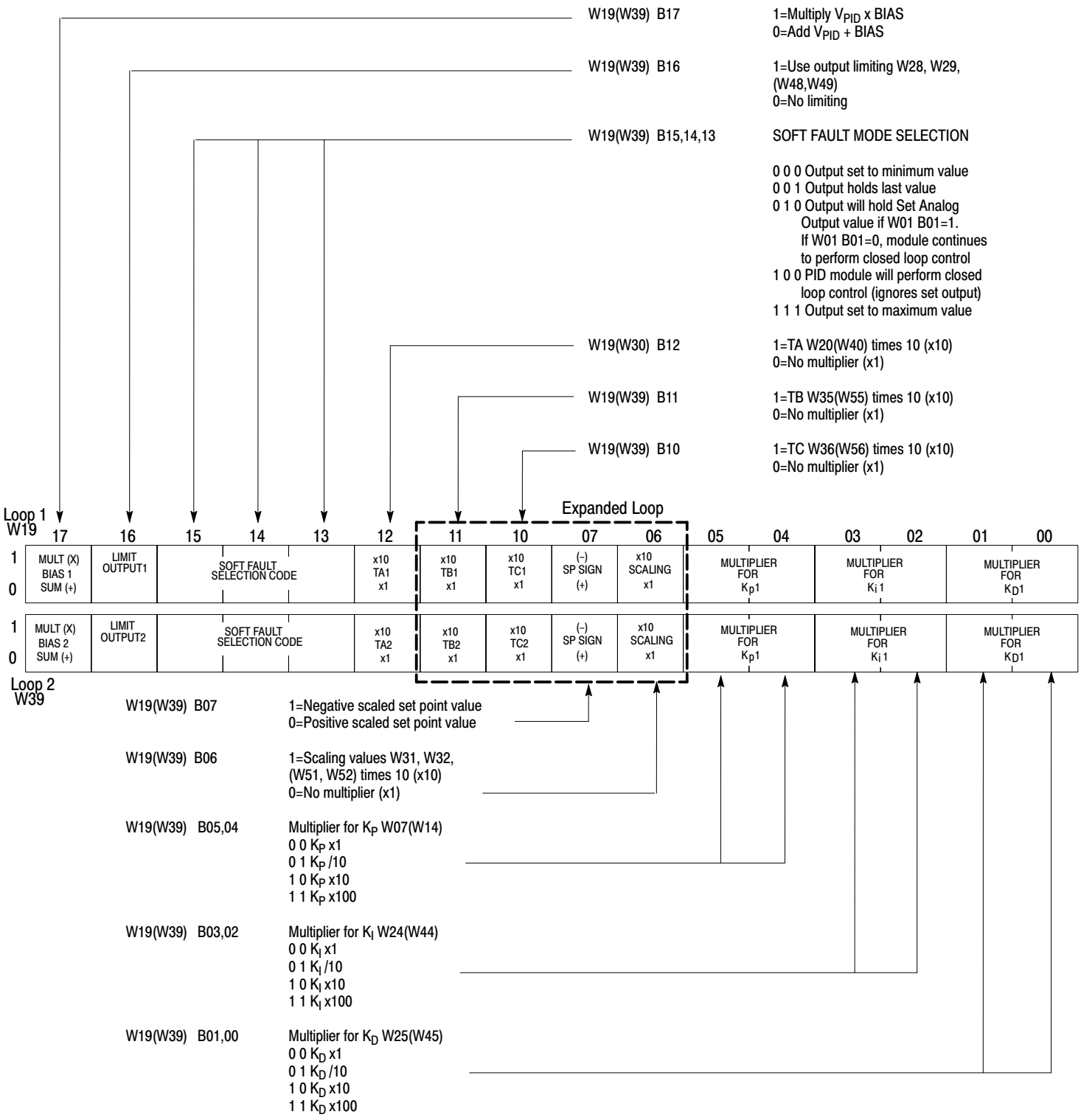
W19 (W39) B15, B14, B13. Soft Fault Mode Selection. These bits select the PID module's response for the loop when communication with the PC processor is broken. The PID module's microprocessor continues to operate and is firmware programmed to respond to the fault. The PID module's STAND-ALONE yellow LED indicator flashes when the module is in the soft fault mode.

NOTE: In order for the PID module to operate in the soft fault mode, the last state witch (switch 1) in the switch group assembly on the I/O chassis backplane must be set to the off position. As such, output of all other modules in the chassis will be de-energized when a major fault is detected by the PC processor.

NOTE: When the PID module enters the soft fault mode, it does not generate a manual request to relinquish control to the auto/manual station. However, if the PID module detects a hardware failure when in soft fault mode it will generate a manual request.

The soft fault operating modes are listed in Table 3.E.

Figure 3.7
Control Word B, Loop 1 W19 and Loop 2 W39



Note: If you change a loop 1 or loop 2 parameter, you must initiate a load/enter sequence

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Table 3.E
Multiplier Codes

W19(W39)			
B15	**B14**	**B13**	**Soft Fault Operating Mode**
0	0	0	Analog output is set to the minimum value (+4mA or +1VDC).
0	0	1	Analog output holds the last value prior to the fault.
0	1	0	The PID module performs closed loop control unless W01 B01 = 1 for loop 1 (W01 B02= 1 for loop 2). If this bit is set prior to the soft fault, the SET OUT value in W05(W12) remains as the loop output.
1	0	0	The PID module performs closed loop control regardless of the status of W01 B01 (B02). If the loop output was the SET OUT value in W05(W12) when the soft fault occurred, the module reverts to PID control. This mode should be selected for interactive PC control.
1	1	1	Analog output is set to the maximum value (+20mA or +5VDC)
Each loop must be set independently. No other codes are permitted.			

W19 (W39) B12 Input Filter Time constant Multiplier. Reset to 0 the multiplier for the input filter time constant TA stored in word W20 (W40) is x1 (no multiplier). Set to 1 the multiplier is x10.

W19 (W39) B11 Lead Time Constant Multiplier. (XF) Reset to 0 the multiplier for the lead time constant TV stored in word W35 (W55) is x1. Set to 1 the multiplier is x 10.

W19 (W39) B10 Lag Time Constant Multiplier. (XF) Reset to 0 the multiplier for the lag time constant TC in word W 36 (W56) is x1. Set to 1 the multiplier is x10.

W19 (W39) B07 Scaled Set Point Sign. (XF) Reset to 0 the set point value in word W06 (W13) is positive. Set to 1 the value is negative. This bit has meaning only when set point scaling has been selected by 16 = 1 in word W30 (W50).

W 19 (W39) B06 Scaling Word Multiplier. (XF) This bit selects the multiplier for the following words:

set point in word W06(W13)
minimum scaling value in word W31(W51)
maximum scaling value in word W32(W52)
loop error in word W62(W69)
read process variable in word W65(W72)

When this bit is reset to 0, the above values are multiplied x1. When set to 1, the values in words W31(W51) and W32(W52) are multiplied x10. The other words are multiplied x 10 only if the values are scaled.

NOTE: The multiplier bit B06 must be examined to determine the correct value of the loop error in word W62(W69) or the read process variable in word W65(W72) when either word is read by the PC processor.

W19(W38)B05, B04 Proportional Gain Multiplier. These two bits select the multiplier for the integral gain K_I in word W24(W44)(table 3.F).

W19(W39) B03, B02 Integral Gain Multiplier. These two bits select the multiplier for the integral gain K_I in word W24(W44) (Table 3.F).

Table 3.F
Multiplier Codes

K_P K_I K_D K_F	W19(W39) W19(W39) W19(W39) W30(W50)	B05 B03 B01 B07	B04 B02 B00 B06	Multiplier
		0 0 1 1	0 1 0 1	X1 /10 x10 x100

W19(W39)B01, B00 Derivative Gain Multiplier. These two bits select the multiplier for the derivative gain K_D in word W25(W45)(Table 3.F).

W20(W40)Input Filter Time Constant, TA. This word contains the time constant for the input digital filter. The digital filter is the equivalent of a single pole low pass filter. Data format is 4-digit BCD (99.99) with

an implied decimal point. the x10 multiplier bit is B12 in word W19(W39). Range is 00.10 to 999.9. a value of zero implies no filter.

W21 (W41) Maximum Negative Error, EMN. This word contains the maximum negative error for the loop. This value can be used for alarm purposes and/or limiting. The alarm condition is indicated by W61(W68)B15. error limiting is selected by B12 = 1 in word W18(W38). Data format is 4-digit BCD with a range from 0000 to 4095. a negative value is implied.

W22(W42) Maximum Positive Error, EMP. This word contains the value used as the maximum positive error for the loop. This value can be used for alarm purposes and/or limiting. The alarm condition is indicated by W61(W68)B14. Error limiting is selected by B12 = 1 in word W18(W38). Data format is 4-digit BCD with a range from 0000 to 4095. a positive value is implied.

W23(W43) Dead Band, DB. This word contains the error dead band value. This value can be used for alarm purposes and/or setting the dead band range. The error dead band extends above and below zero error so that the dead band range is twice the dead band value. Dead band is selected by B11 = 1 in word W18(W38). The alarm condition is indicated by W61(W68)B11. Data format is 4-digit BCD with a range from 0000 to 4095 above and below zero error.

Any time the error value is outside the dead band, the actual error value will be used for computational purposes. As it crosses into the dead band, the error value continues to be used for computational purposes until it crosses zero. Once it crosses zero and as long as it remains in the dead band, the error value will be set to zero for computational purposes.

W24(W44) Integral Gain, K I (Reset Term 1/T I). If W02B00 is reset, the module uses the A-B value K I and this word contains the integral gain constant for the loop. If W02 B00 is set, the module uses the ISA value I/T I and the word contains the reset term for the loop. Data format is 4-digit BCD, 9.999 in units of inverse seconds (A-B) or inverse minutes (ISA), with implied decimal point. Multiplier bits W19(W39)B03, B02 can be selected for x1, divided by 10, x10, x100 (Table 3.F). By using multipliers, the range can be extended from .0000 to 999.9.

The integral term K I or reset term 1/T I must be greater than zero for the module to perform bumpless transfer. Reset or hold the integral term V I to zero by setting K I or 1/T I = 0.

W25(W45) Derivative Gain, K D (Rate Term, Td). If W02 B00 is reset, the module uses the A-B value K D and this word contains the derivative gain constant for the loop. If W02 B00 is set, the modules uses the ISA value Td and this word contains the rate term for the loop. Data format is 4-digit BCD, 99.99 in units of seconds (A-B) or minutes (ISA), with implied decimal point. Multiplier bits W19(W39)B03, B02 can be selected by 1, divided by 10, x10, x100 (Table 3.F). By using multipliers, the range can be extended from 0.000 to 9999.

W26(W46) Integral Term Limit, V I MAX. This word contains the integral term limit for the loop. It can be used for alarm purposes and/or limiting. The alarm condition is indicated by W61(W68)B10. Integral term limiting is selected by B10 = 1 in word W18(W38). Data format is 4-digit BCD with a range from 0000 to 9999.

NOTE: When limiting is selected, lowering the value of V I MAX reduces the PID module's ability to adjust the integral term. The performance of bumpless transfer could be hindered.

W27(W47) Derivative Term Limit, VD MAX. This word contains the derivative term limit for the loop. It can be used for alarm purposes and/or limiting. The alarm condition is indicated by W61(W68)B02. Derivative term limiting is selected by B02 = 1 in word W18(W38). Data format is 4-digit BCD with a range from 0000 to 9999.

W28(W48) Minimum Output Limit, VMIN. This word contains the minimum limit for the analog output that is determined by the PID module's algorithm. This value can be used for alarm purposes and/or limiting. The alarm condition is indicated by W61(W68)B01. Output limiting is selected by B16 = 1 in word W19(W39). Data format is 4-digit BCD with range from 0000 to 4095. This limit has no effect on a SET OUT value downloaded from the PC processor into word W05(W12).

W29(W49) Maximum Output Limit, VMAX. This word contains the maximum limit for the analog output that is determined by the PID module's algorithm. This value can be used for alarm purposes and/or limiting. The alarm is indicated by W61(W68)B00. Output limiting is selected by B16 = 1 in word W19(W39). Data format is 4-digit BCD with a range from 0000 to 4095. This limit has no effect on a SET OUT value downloaded from the PC processor into word W05(W12).

NOTE: The following words, W30(W50) through W36(W56), can be programmed if the expanded features (XF) of the loop are selected by

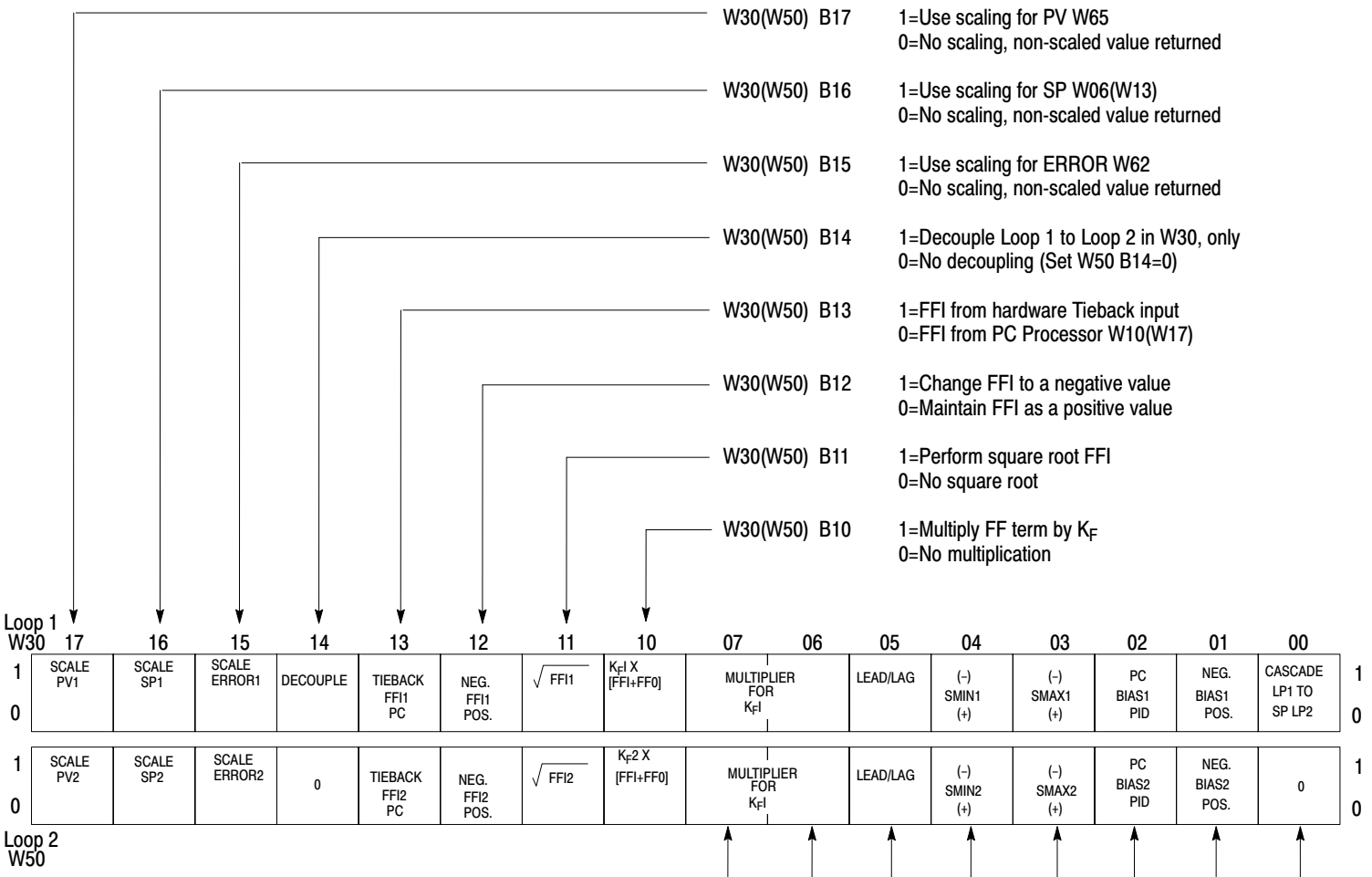
W01 B14 = 1. The values of features not used must be zero. Section 3.6 describes expanded features such as cascade, decouple and feedforward.

W30(W50) Expanded Control Word (XF) This word together with loop control word A, W18(W38), and loop control word B, W19(W39), select the configuration for the loop. The expanded loop features are active when selected by W01 B14 = 1. Bits 17 through 00 of the expanded control word are defined below and summarized in Figure 3.8 for loop 1 word W30 and loop 2 word W50.

W30(W50)B17 Process Variable Scaling. (XF) Reset to 0 inhibits process variable scaling. Set to 1 enables the scaling limits SMIN and SMAX in words W32(W51) and W32(W52) respectively to determine the scaled value of the process variable. The scaled or unscaled process variable will be read by the PC processor in word W65(W72). Refer to section titled Scaling for additional information about scaling.

W30(W50)B16 Set Point Scaling. (XF) Rest to 0 inhibits set point scaling. Set to 1 the module interprets this word as a scaled value based on the scaling limits SMIN and SMAX IN WORD W32(W51) and W32(W52), respectively. Refer to section titled Scaling for additional information about scaling.

Figure 3.8
Expanded Control Word, Loop 1 W30 and Loop 2 W50



W30(W50)B15 Error Scaling. (XF) Reset to 0 inhibits loop error scaling. Set to 1 enables the scaling limits SMIN and SMAX in words W31(W51) and W32(W52) respectively to determine the scaled value of the loop error. The scaled or unscaled loop error will be read by the PC processor in word W62(W69). Refer to section titled scaling for additional information about scaling.

W30(W50)B14 Decouple. (XF) Reset to 0 inhibits decoupling. Set to 1 enables decoupling. The loop 1 PID calculation VPID 1 is used for the feedforward input FFI to the loop 2 control algorithm. Decoupling overrides the feedforward input FFI for loop 2. (W50 B14 for loop 2 must be reset to 0.) Refer to section titled Closed Loop Control for additional information about decoupling.

W30(W50)B13 Source of Feedforward Input, FFI. (XF) Reset to 0 selects the value in word W10(W17) as the feedforward input for the loop. Set to 1 selects the tieback input as the feedforward input.

W30(W50)B12 Feedforward Input Sign. (XF) Reset to 0 maintains the positive value of the feedforward input for the loop. Set to 1 changes the value to negative.

W30(W50)B11 Feedforward Input Square Root. (XF) Reset to 0 inhibits the square root function. Set to 1 enables the normalized square root of the feedforward input, (square root of FFI) x (square root of 4095). Square root allows the linearization of differential pressure type flow transducers.

W30(W50)B10 Feedforward Term Multiplication. (XF) Reset to 0 inhibits multiplication. Set to 1 enables the feedforward term (feedforward offset + feedforward input) to be multiplied by the feedforward gain in word W34(W54). The result is K_F x (FFO + FFI).

W30(W50)B07, 06 Feedforward Gain Multiplier. (XF) These two bits select the multiplier for feedforward gain K_F in word W34(W54)(Table 3.F).

W30(W50)B05 Lead/Lag. (XF) Reset to 0 inhibits the lead/lag function. Set to 1 enables the lead/lag function. The values for the lead and lag time constants are contained in words W35(W55) and W36(W56), respectively. Refer to section titled Lead/Lag Filter for additional information about the lead/lag filter.

W30(W50)B04 Minimum Scaling Sign. (XF) Reset to 0 the sign for SMIN in word W32(W51) is positive. Set to 1 the sign is negative.

W30(W50)B03 Maximum Scaling Sign. (XF) Reset to 0 the sign for SMAX in word W32(W52) is positive. Set to 1 the sign is negative.

W30(W50)B02 Source of Bias. (XF) Reset to 0 the feedforward value is the loop bias. Set to 1 the bias value in word W08(W15) is the loop bias.

W30(W50)B01 Bias (FFV) Sign. (XF) Reset to 0 the sign of the feedforward/bias term remains the same. Set to 1 the sign is reversed.

W30(W50)B00 Cascade. (XF) Reset to 0 inhibits the cascade feature. Set to 1 cascades the calculated output of loop 1 into the set point of loop 2. (W50 B00 for loop 2 must be reset to 0). Refer to section titled Closed Loop Control for additional information about cascading.

W31(W51) Minimum Scaling Value SMIN. (XF) This word contains the minimum (or bottom) scale value of the loop scaling algorithm. This value is in engineering units. Data format is 4-digit BCD (9999 maximum). The sign bit B04 in word W30(W50) and the x10 multiplier bit B06 in word W19(W39) must be considered to determine the value. The range can be $\pm$99990. Refer to section titled Scaling for additional information about scaling.

W32(W52) Maximum Scaling Value, SMAX. (XF) This word contains the maximum (or top) scale value of the loop scaling algorithm. This value is in engineering units. Data format is 4-digit BCD (9999 maximum). The sign bit B03 in word W30(W50) and the x10 multiplier bit B06 in word W19(W39) must be considered to determine the value. The range can be $\pm$ 99990. refer to section titled Scaling for additional information about scaling.

W33(W53) Feedforward Offset, FFO. (XF) This word contains the feedforward offset of the loop. It is added to the feedforward input. Data format is 4-digit BCD (9999 maximum).

W34(W54) Feedforward Gain, K F. (XF) This word contains the feedforward gain constant for the loop. Data format is 4-digit BCD (99.99 dimensionless with implied decimal point. Multiplier bits B07, B06 in word W30(W50) can be selected for x1, divided by 10, x10, 1100 (Table 3.F). The range can be 0.000 to 9999 when using the multipliers.

W35(W55) Lead Time Constant, TB. (XF) This word contains the lead time constant for the loop. The lead/lag feature is selected by bit B05 in word W30(W50). To disable the lead portion of the filter, reset TB to zero. Data format is 4-digit BCD (99.99 in units of seconds) with implied decimal point. By using the x10 multiplier bit B11 in word W19(W39), the range can be 00.00 to 999.9.

W36(W56) Lag Time Constant, TC. (XF) This word contains the lag time constant for the loop. The lead/lag feature is selected by bit B05 in word W30(W50). To disable the lag portion of the algorithm, reset TC to zero. Data format is 4-digit BCD (99.99 in units of seconds) with implied decimal point. By using the x10 multiplier bit B10 in word W19(W39), the range can be 00.00 to 999.9.

NOTE: There is no word number 37 to program. By omitting W37, the storage words for loop 1 and loop 2 parameters are exactly 20 counts apart.

Example: W20 Integral Gain 1 (W40 Integral Gain 2)

Status Block: W57-W74

The status block is a read block transfer file of up to 18 words which is used to report loop status, alarm and diagnostic information and to prompt the proper block transfer sequences.

Only words W57 through W67 will be read if the module is selected for loop 1 operation. The entire block (words W57 through W74) is read if the module is selected for two-loop operation.

The 18 words that comprise the status block are defined in the paragraphs that follow. Table 3.G lists the status block words. All the words of the dynamic block, loop block and status block are listed in Table 3.J, in Figure 3.13 and Figure 3.14 found at the end of section titled Word and Bit Definitions.

Table 3.G
Status Block Words

Word	Title	Abbreviation
Both Loops		
W57	For future use	
W58	Alarm	
W59	Next Block Start Address	
W60	Loop Time/Diagnostic	
Loop 1		
W61	Loop 1 Status	
W62	Loop 1 Error	ERROR1
W63	Read Loop 1 Output	READ V1
W64	Read Analog Input 1	READ IN1
W65	Read Process Variable 1	READ PV1
W66	Read Tieback Input 1	READ TIE1
W67	Read Feedforward Value 1	READ FFV1
Loop 2		
W68	Loop 2 Status	
W69	Loop 2 Error	ERROR2
W70	Read Loop 2 Output	READ V2
W71	Read Analog Input 2	READ IN2
W72	Read Process Variable 2	READ PV2
W73	Read Tieback Input 2	READ TIE2
W74	Read Feedforward Value 2	READ FFV2

W57 This word is reserved for future use. It will contain 0000.

W58 Alarm Word. This word contains alarm information for both loops. It contains information concerning possible programming errors and operating faults. Specific loop faults are found in the status word W61 for loop 1 (W68 for loop 2). Bits 17 through 00 of alarm word W58 are defined below and summarized in Figure 3.9.

W58 B17, B16 Block Identifiers. These two bits identify the status block. Both bits will be read as 0 by the PC processor.

W58 B15 Dynamic Block Error. Set to 1 the previously transferred dynamic block contained a programming error. To identify the error, W01 B07 must be set to 1 so that the loop time/diagnostic word W60 can report diagnostic information. The upper byte of W60 will contain the dynamic block error code. See word W60 below for additional information.

W58 B14 Loop Block Error. Set to 1 the previously transferred loop 1 or loop 2 block contained a programming error. To identify

the error, W01 B07 must be set to 1 so that the loop time/diagnostic word W60 can report diagnostic information. The lower byte of W60 will contain the error code. See word W60 below for additional information.

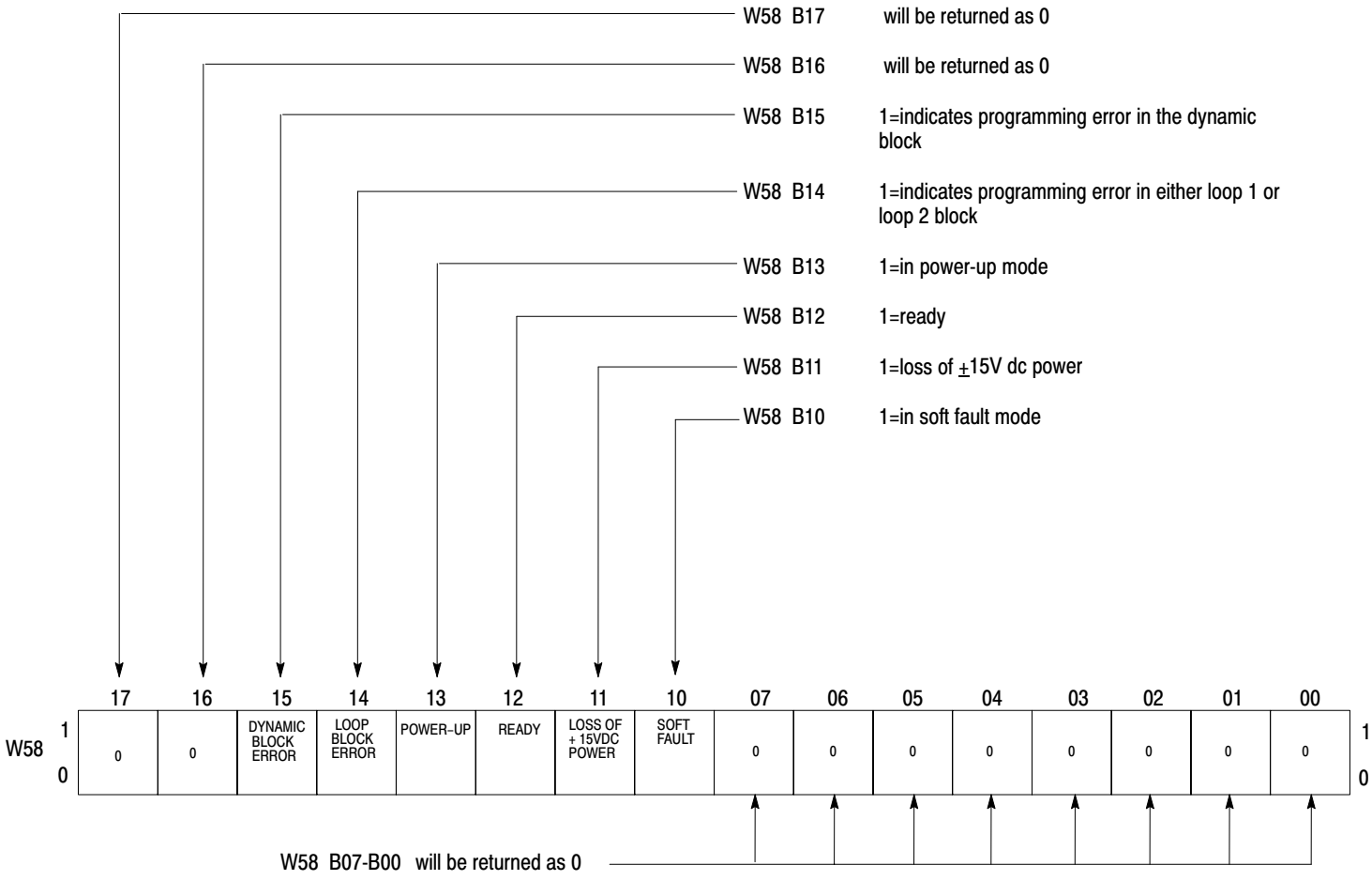
W58 B13 Power-Up. After the PID module has received the first valid dynamic block with the load bit W01 B06 =1, this bit will be reset to 0. Note that this does not mean that the PID module is programmed, only that the first dynamic block has been processed.

After the PID module has gone through its initial power-up procedure or after the restoration of +5VDC, it will set bit W58 B13 to 1. This occurs when the module has cleared all internal memory and is waiting to be programmed by block transfers to complete the initial load/enter sequence. See section titled Power-Up Load/Enter Sequence for additional power-up load/enter sequence information.

W58 B12 Ready. Set to 1 indicates that the load portion of the load/enter sequence has been successfully completed. The ready bit should be used to initiate the setting of the enter bit to complete the sequence. After the enter bit is received by the PID module, the ready bit will be reset to 0.

Before the enter bit is received by the PID module, a ready bit status of 0 indicates an error was detected in either the dynamic block or a loop block during the load portion of the load/enter sequence. The error must be corrected before the ready bit can be set to 1. See section titled Load/Enter Sequence or additional Load/enter sequence information.

Figure 3.9
Alarm Word W58



11112

W58 B11 Loss of +15VDC. Reset of 0 indicates that power is present. Set to 1 indicates that the external +15VDC power is not present. When +15VDC power is lost, the PID module generates a manual request by closing the contact output.

W58 B10 Soft Fault Mode. Reset to 0 indicates that module is in the normal operating mode. Set to 1 indicates the PID module is operating in the soft fault mode. The soft fault response is programmed by W19(W39) B15,14,13 (Table 3.E). Soft fault reset is accomplished by setting W01 B10 to 1.

W58 B07 through B00. These bits are reserved for future use and will be reset to 0.

W59 Next Block Start Address. The PID module controls the block transfer programming sequences by determining which block should be transferred next. This word contains the data table address of the first word in the file associated with the next write block transfer. The PID module reports to the PC processor the block start addresses programmed in word W03 for the dynamic block, in word W04 for the loop 1 block, or in word W11 for the loop 2 block. The PID module performs no data manipulation on the next block start address in word W59.

W60 Loop Time/Diagnostic. This is a dual function word. This word can report either the loop update time or diagnostic information. Its function is established by W01 B07. When W01 B07 = 0, W60 reports loop time. When W01 B07 = 1, W60 reports diagnostic information (Figure 3.10).

When reporting loop time, the data format is 0-100 milliseconds. Bit W60 B17 will be set to 1 to indicate when this word is reporting loop time. The loop update time is nominally 100msec. The loop update time is the time between successive module scans of the analog inputs. Only one block transfer will be allowed during a loop update (Figure 3.11).

When reporting diagnostics, two separate error codes can be reported. The error code is a 2-digit BCD value. The upper byte will indicate a dynamic block error code. The lower byte will indicate a loop block error code. If more than one error code exists, the first error code will be displayed until it is corrected. Then the next error code will be displayed. Table 3.H and Table 3.I contain error code definitions.

W61(W68) Loop Status. This word indicates various alarm conditions for the corresponding loop and contains sign information for certain status block words. Bits 17 through 00 of the loop status word are defined below and summarized in Figure 3.12 for loop 1 word W61 and loop 2 word W68.

Figure 3.10
Loop Time/Diagnostic Word W60

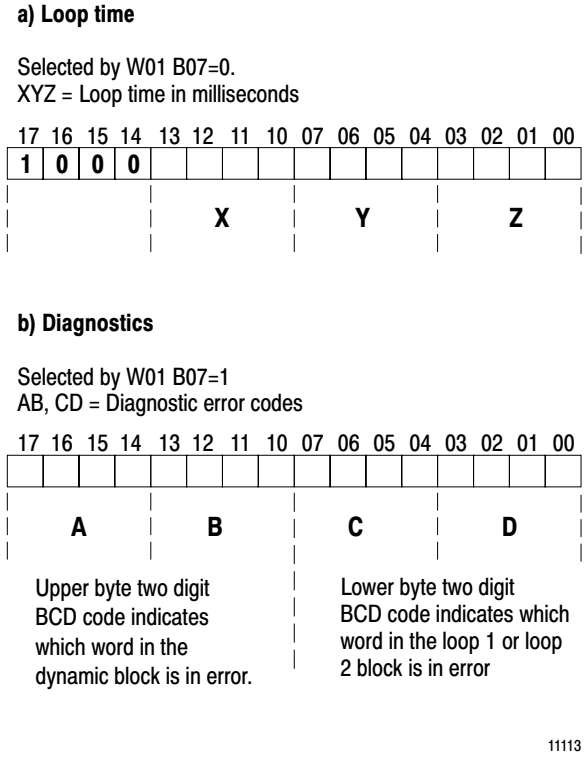


Figure 3.11
Loop Update Time

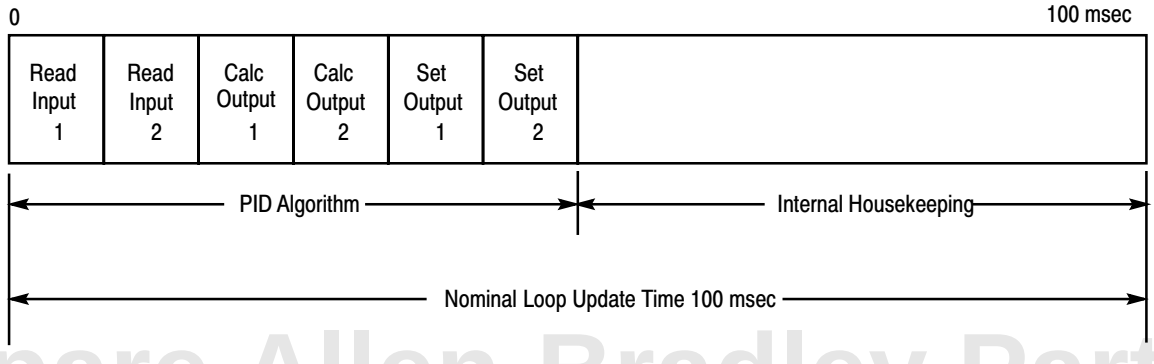


Table 3.H
W60 Upper Byte Programming Error Codes

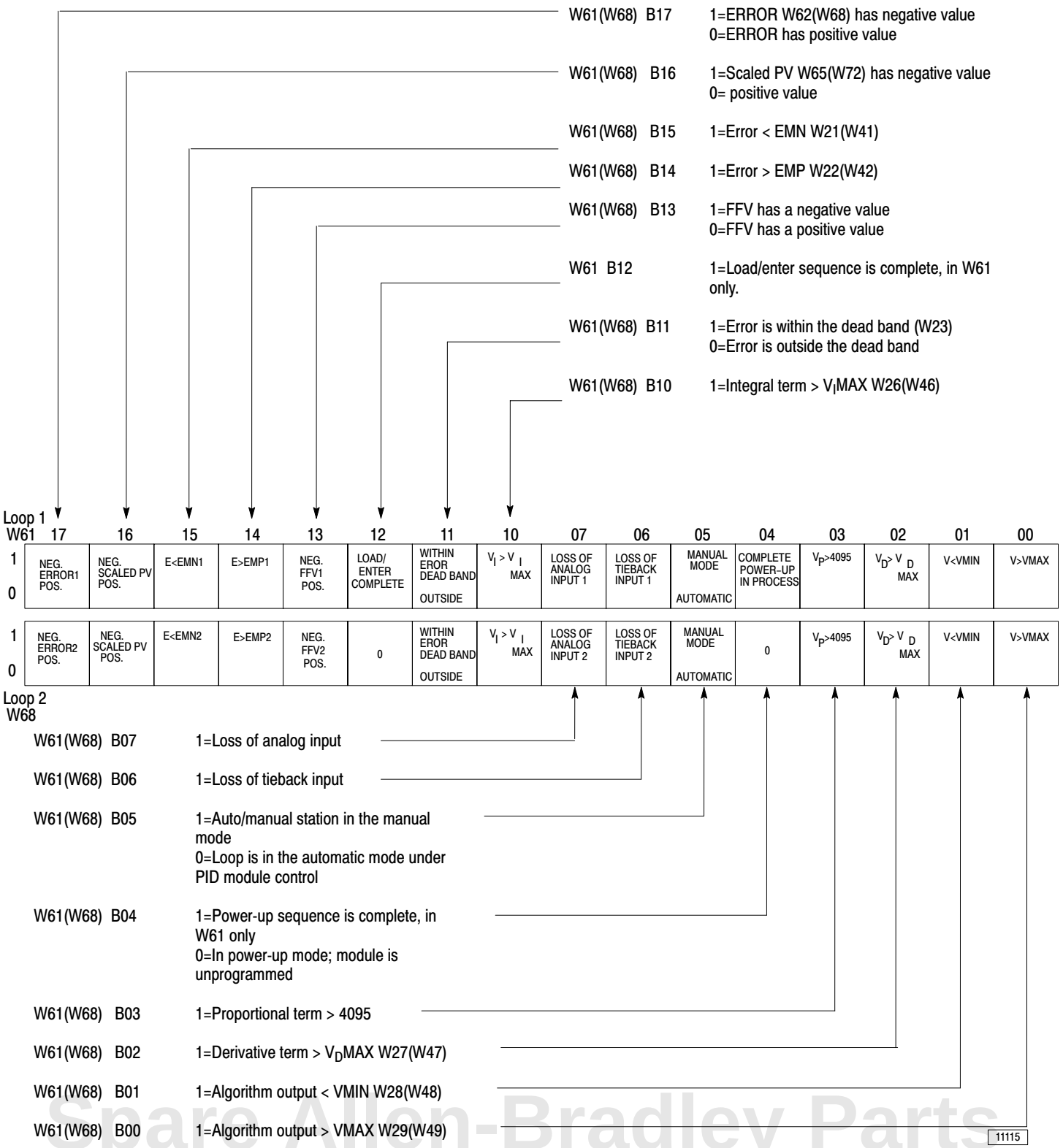
BCD Code	Dynamic Block Word Errors
01	Incorrect number of words for the dynamic block (1-loop or 2-loop configuration)
02	Not currently used as error code.
03	Not currently used as error code.
04	Not currently used as error code.
05	W05 is above maximum or has illegal BCD value.
06	W06 has illegal BCD value.
07	W07 has illegal BCD value.
08	W08 has illegal BCD value.
09	W09 has illegal BCD value.
10	W10 has illegal BCD value.
11	Not currently used as error code.
12	W12 is above maximum or has illegal BCD value.
13	W13 has illegal BCD value.
14	W14 has illegal BCD value.
15	W15 has illegal BCD value.
16	W16 has illegal BCD value.
17	W17 has illegal BCD value.
BCD Code	**Dynamic Block Word Errors**
60	Less than 10 words transferred (1-loop configuration)
61	Less than 17 words transferred (2-loop configuration).
62	Dynamic block identifier bits B17, B16 are not set correctly in W01, and/or W18, and/or W38.
63	Less than 13 words transferred (1 loop configured with SET OUT value of loop 2 requested).
64	Read and write block transfers are out of sequence. Status block must be transferred first.
65	The load bit and enter bit must be set concurrently.
66	The enter bit must not be set before the ready bit is returned
67	The verify and load bits must not be set concurrently.
68	During the power-up load/enter sequence, the enter bit must be set to complete the sequence.
69	During the load portion of the power-up load/enter sequence, the dynamic block can be transferred only once.

Table 3.I
W60 Lower Byte Programming Error Codes

BCD Code	Dynamic Block Word Errors
18	Loop 1 constants block was not transferred in the load/enter sequence.
19	W19 has illegal soft fault code 011, 101, or 110.
20	W20 has illegal BCD value.
21	W21 is above maximum or has illegal BCD value.
22	W22 is above maximum or has illegal BCD value.
23	W23 is above maximum or has illegal BCD value.
24	W24 has illegal BCD value.
25	W25 has illegal BCD value.
26	W26 has illegal BCD value
27	W27 has illegal BCD value.
28	W28 is above maximum or has illegal BCD value.
29	W29 is above maximum, has illegal BCD value, or is less than W28.
30	W30 has cascade or decouple selected when only loop 1 is selected.
31	W31 has illegal BCD value.
32	W32 has illegal BCD value or is less than or equal to W31 value..
33	W33 has illegal BCD value.
34	W34 has illegal BCD value.
35	W35 has illegal BCD value.
36	W36 has illegal BCD value.
BCD Code	**Loop 2 Word Errors**
38	Loop 2 constants block was not transferred in the load/enter sequence.
39	W39 has illegal soft fault code o11, 101, or 110.
40	W40 has illegal BCD value.
41	W41 is above maximum or has illegal BCD value.
42	W42 is above maximum or has illegal BCD value.
43	W43 is above maximum or has illegal BCD value.
44	W44 has illegal BCD value.
45	W45 has illegal BCD value.
46	W46 has illegal BCD value.
47	W47 has illegal BCD value.
48	W48 is above maximum or has illegal BCD value.
49	W49 is above maximum, has illegal BCD value, or is less than W48.
50	Not used
51	W51 has illegal BCD value.
52	W52 has illegal BCD value or is less than or equal to W51.
53	W53 has illegal BCD value.
54	W54 has illegal BCD value.
55	W55 has illegal BCD value.
56	W56 has illegal BCD value

BCD Code	Block Transfer Errors
70	Communication Fault. The number of block transfer words exceeds the number expected by PID module.
80	Less than 12 words transferred in the standard loop constant block.
81	Less than 19 words transferred in the expanded loop constants block.
82	Loop 1 or loop 2 constants block can be transferred only in a load/enter sequence.

Figure 3.12
Loop Status Word, Loop 1 W61 and Loop 2 W68



W61(W68)B17 Sign of Loop Error. Reset to 0 the sign of the error value in word W62(W69) is positive. Set to 1 the sign is negative.

W61(W68)B16 Sign of Read Process Variable. Reset to 0 the sign of the scaled process variable in word W65(W72) is positive. Set to 1 the sign is negative. This bit has meaning only when process variable scaling has been selected by W30(W50)B17 = 1.

W61(W68)B15 Error <Maximum Negative Error. Reset to 0 the error value is greater than or equal to the maximum negative error EMN in word W21(W41). Set to 1 the loop error is less than the maximum negative error. The bit status is reported whether or not error limiting is selected.

W61(W68)B14 Error>Maximum Positive Error. Reset to 0 the error value is less than or equal to the maximum positive error EMP in word W22(W42). Set to 1 the loop error is greater than the maximum positive error. The bit status is reported whether or not error limiting is selected.

W61(W68)B13 Sign of Feedforward Value. Reset to 0 the sign of the feedforward value in word W67(W74)is positive. Set to 1 the sign is negative.

W61(W68)B12 Load/Enter Complete. Reset to 0 when the module receives a dynamic block transfer with the load bit W01 B06 = 1. Bit B12 will be set to 1 at the completion of the load/enter sequence after the module successfully processes the dynamic block with the enter bit W01 B03 =1. The bit will remain set to 1 until a new load/enter sequence is attempted. (W68 B12 in loop 2 will be returned as 0.) Refer to sections titled Power-Up Load/Enter Sequence and Load/Enter Sequence for additional information.

W61(W68)B11 Error within Dead Band. Reset to 0 the error for the loop is outside the dead band established by the value in word W23(W43). Set to 1 the error is inside the dead band. The bit status is reported whether or not the dead band feature is selected.

NOTE: When the error enters the dead band range, the bit will not be set until the error reaches (crosses) zero. It will be reset when the error exceeds the dead band value.

W61(W68)B10 Integral Term>Integral Term Limit. Rest to 0 the integral term V I is less than or equal to the integral term limit V I MAX in word W26(W46). Set to 1 the integral term is greater than V I MAX. The bit status is reported whether or not integral term limiting is selected.

W61(W68)B07 Loss of Analog Input. Rest to 0 the analog input signal from an input device is present and can be found in word W64(W71). Set to 1 the hardware analog input is less than the minimum value of +4mA or 1VDC. A loss of hardware analog input will be detected whether or not a PV value is downloaded from the PC processor into word W09(W16).

The loss of a hardware analog input will cause the corresponding loop output to be held at its last value until the input is restored. However, if the process variable has been downloaded from the PC processor into word W09(W16), loss of a hardware analog input will be detected but will not cause the analog output to be held.

NOTE: When downloading PC values from the PC processor when an input device is not connected, jumper the INPUT (+LEAD) terminal to the +15VDC terminal to prevent the loss of input bit W61(W68)B07 from being set.

NOTE: Loss of input detection when analog inputs are configured in voltage mode requires the use of 10K ohm 1/4 watt resistor. The resistor must be connected between the INPUT (+LEAD) and (-LEAD) terminals to ensure loss of input detection for an open or short circuit in one or both leads of the input device. The module input impedance is thereby reduced to 10k ohms. A resistor is not required for loss of input detection for current mode analog inputs.

If either decoupling or cascading is selected and the hardware analog input to loop 1 is lost, the output for both loops will be held regardless of the status of the loop 2 inputs.

The loss of a hardware analog input is indicated by bit B07 of loop status word W61(W68) and bit B02 of the status monitor byte.

W61(W68)B06 Loss of Tieback Input. Reset to 0 indicates that the tieback input signal is present and can be found in word W66(W73). Set to 1 indicates that the input is less than the minimum value of +4mA or +1VDC.

The loss tieback input will cause the corresponding loop output to be held at its last value until the input is restored.

If either decoupling or cascading is selected and the tieback input to loop 1 is lost, the output for both loops will be held regardless of the status of the loop 2 inputs.

When the tieback input is used as a hardware analog input, loss of input detection does not require the use of an external resistor.

The loss of a tieback input is indicated by bit B06 or loop status word W61(W68) and bit B02 of the status monitor byte.

W61(W68)B05 Manual Mode. Reset to 0 indicates that the PID module is controlling the analog output signal to the actuator. Set to 1 indicates that the module has relinquished control to the user supplied auto/manual station, placing the station in the manual mode. Manual operation could have been initiated at the auto/manual station by the loss of analog power, or by setting W01 B00 to 1.

W61(W68)B04 Power-Up Complete. Rest to 0 at power-up. After a valid power-up load/enter sequence initializes the module, this bit is set to 1. (W68 B04 for loop 2 will be reset.) Refer to section titled Load/Enter Sequence for additional information.

W61(W68)B03 Proportional Term>4095. Reset to 0 indicates that the proportional term V_P for the loop is less than or equal to 4095 (full scale). Set to 1 indicates that V_P is greater than 4095.

W61(W68)B02 Derivative Term>VD MAX. Reset to 0 indicates that the derivative term VD for the loop is less than V_D MAX. Set to 1 indicates that V_D is greater than V_D MAX IN W27(W47).

W61(W68)B01 ALGORITHM OUTPUT<Minimum Output. Reset to 0 indicates that the analog output is in range and greater than or equal to the minimum output value VMIN in word W28(W48). Set to 1 indicates that the analog output computed by the PID module is less than the VMIN. The bit status is reported whether or not output limiting has been selected. This status bit does not monitor a SET OUT value downloaded from the PC processor into word W05(W12).

W61(W68)B00 Algorithm Output>Maximum Output. Reset to 0 indicates that the analog output is in range and less than or equal to the maximum output value VMAX in word W29(W49). Set to 1 indicates that the analog output computed by the PID module is greater than VMAX. The bit status is reported whether or not output limiting has been selected. This status bit does not monitor a SET OUT value downloaded from the PC processor into word W05(W12).

W62(W69) Loop Error, ERROR. This word contains the loop error. Data format is 4-digit BCD. The sign bit B17 in word W61(W668) can establish an unscaled range of 0 to ±4095.

When error scaling is selected by W30(W50)B15 = 1, the loop error can be reported in user-selected engineering units. The sign bit B17 in word W61(W68) and the x 10 multiplier bit B06 in word W19(W39) must be examined to determine the value. The scaled range can be ±99990. Refer to section titled Scaling.

W63(W70) Read Loop Output, READ V. This word contains the final analog output value as determined by the module's PID algorithm. Data format is 4-digit BCD or 12-bit binary. Format is selected by W01 B12. Range is 0000 to 4095.

NOTE: When a SET OUT value is downloaded from the PC processor into word W05(W12) by setting W01 B01(W01 B02) = 1, the SET OUT value will override the analog output value. However, the value reported in W63(W70) will always be the analog output value as determined by the module's PID algorithm, not the SET OUT value.

W64(W71) Read Analog Input, READ IN. This is the actual input value read by the analog-to-digital converter in the module. Data format is 4-digit BCD or 12-bit Binary. Format is selected by W01 B12. Range is 0000 to 4095.

W65(W72) Read Process Variable, READ PV. This is the actual process variable used by the PID module. Data format is 4-digit BCD. The unscaled range is 0000 to 4095.

When process variable scaling is selected by W30(W50)B17 = 1, READ PV can be reported in user-chosen engineering units. The sign bit B16 in word W61(W68) and the x10 multiplier bit B06 in word W19(W39) must

be examined to determine the value. The range can be ±99990. Refer to section titled Scaling.

W66(W73) Read Tieback Input, READ TIE. This is the actual value read by the analog-to-digital converter in the module. Data format is 4-digit BCD or 12-bit binary. Format is selected by W01 B12. Range is 0000 to 4095.

W67(W74) Read Feedforward Value, Read FFV. This is the feedforward computation as performed by the PID module. Data format is 4-digit BCD with sign bit B13 in word W61(W68) allowing a range of ±9999.

Control and status words are summarized in Figure 3.13, Figure 3.14 and Table 3.J.

Figure 3.13
Control Word Summary

Master Control Word W01

	17	16	15	14	13	12	11	10	07	06	05	04	03	02	01	00	
1	1	1	LOOP 1	EXPANDED	CALIB	BINARY	BINARY SP	SOFT FAULT RESET	DIAG	LOAD	VERIFY CODE		ENTER	SET OUTPUT 2	SET OUTPUT 1	MANUAL REQUEST	1
0			2 LOOPS	STANDARD		BCD	BCD		LOOP TIME		0	0					0

Loop 1 Control Word A W18

1	0	1	PC PV1 PID	$\sqrt{\text{PV1}}$	PV-SP ERROR1 SP-PV	LIMIT ERROR1	DEAD BAND	V1 MAX LIMIT	PROPORTIONAL ERROR FUNCTION	INTEGRAL ERROR FUNCTION	PV DERIV. ERR. Error	VD MAX LIMIT	HOLD PID1	HOLD BIAS1	1
0															0

Loop 1 Control Word B W19 — Expanded Loop

1	MULT (X) BIAS 1 SUM (+)	LIMIT OUTPUT1	SOFT FAULT SELECTION CODE	x10 TA1 x1	x10 TB1 x1	x10 TC1 x1	(–) SP SIGN (+)	x10 SCALING x1	MULTIPLIER FOR K_P1	MULTIPLIER FOR K_I1	MULTIPLIER FOR K_D1	1
0												0

Expanded Loop 1 Control Word W30

1	SCALE PV1	SCALE SP1	SCALE ERROR1	DECOUPLE	TIEBACK FFI1 PC	NEG. FFI1 POS.	$\sqrt{\text{FFI1}}$	K_FI X [FFI+FF0]	MULTIPLIER FOR K_FI	LEAD/LAG	(–) SMIN1 (+)	(–) SMAX1 (+)	PC BIAS1 PID	NEG. BIAS1 POS.	CASCADE LP1 TO SP LP2	1
0																0

Loop 2 Control Word A W38

1	1	0	PC PV2 PID	$\sqrt{\text{PV2}}$	PV-SP ERROR2 SP-PV	LIMIT ERROR2	DEAD BAND	V1 MAX LIMIT	PROPORTIONAL ERROR FUNCTION	INTEGRAL ERROR FUNCTION	PV DERIV. ERR. Error	VD MAX LIMIT	HOLD PID2	HOLD BIAS2	1
0															0

Loop 2 Control Word B W39 — Expanded Loop

1	MULT (X) BIAS 2 SUM (+)	LIMIT OUTPUT2	SOFT FAULT SELECTION CODE	x10 TA2 x1	x10 TB2 x1	x10 TC2 x1	(–) SP SIGN (+)	x10 SCALING x1	MULTIPLIER FOR K_P1	MULTIPLIER FOR K_I1	MULTIPLIER FOR K_D1	1
0												0

Expanded Loop 2 Control Word W50

1	SCALE PV2	SCALE SP2	SCALE ERROR2	0	TIEBACK FFI2 PC	NEG. FFI2 POS.	$\sqrt{\text{FFI2}}$	K_F2 X [FFI+FF0]	MULTIPLIER FOR K_FI	LEAD/LAG	(–) SMIN2 (+)	(–) SMAX2 (+)	PC BIAS2 PID	NEG. BIAS2 POS.	0	1
0																0

Note: If you change a loop 1 or loop 2 parameter, you must initiate a load/enter sequence.

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Figure 3.14
Status Word Summary

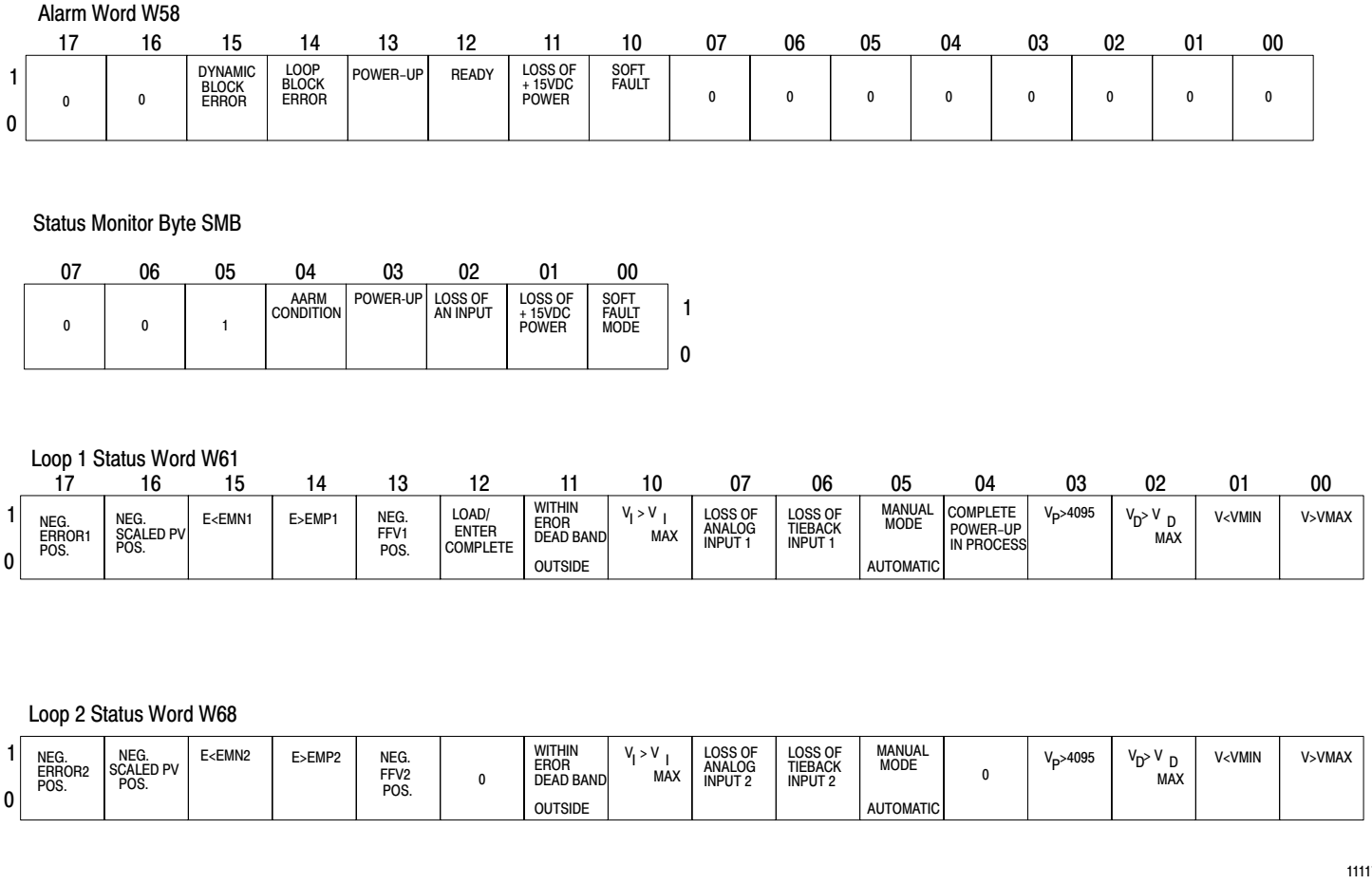


Table 3.J
Word Summary

DYNAMIC BLOCK			**STATUS BLOCK**		
W01	Master Control Word		W57	For Future Use	
W02	Control Word		W58	Alarm (both loops)	
W03	Dynamic Block Start Address		W59	Next Block Start Address	
			W60	Loop Time/Diagnostic	
W04	Loop 1 Block Start Address		W61	Loop 1 Status	
W05	Set Analog Output 1	SET OUT1	W62	Loop 1 Error	ERROR1
W06	Set Point 1	SP1	W63	Read Loop 1 Output	READ V1
W07	Proportional Gain 1	K_P1	W64	Read Analog Input 1	READ IN1
W09	Bias 1	BIAS 1	W65	Read Process Variable 1	READ PV1
W09	Set Process Variable 1	SET PV1	W66	Read Tieback Input 1	READ TIE1
W10	Set Feedforward Input 1	SET EFFI1	W67	Read Feedforward Value 1	READ FFV1
			W68	Loop 2 Status	
W11	Loop 2 Block Start Address		W69	Loop 2 Error	ERROR2
W12	Set Analog Output 2	SET OUT 2	W70	Read Loop 2 Output	READ V2
W13	Set Point 2	SP2	W71	Read Analog Input 2	READ IN2
W14	Proportional Gain 2	K_P2	W72	Read Process Variable 2	READ PV2
W15	Bias 2	BIAS 2	W73	Read Tieback Input 2	READ TIE2
W16	Set Process Variable 2	SET PV2	W74	Read Feedforward Value 2	READ FFV2
W17	Set Feedforward Input 2	SET FFI2			
LOOP 1 BLOCK			**LOOP 2 BLOCK**		
W18	Loop 1 Control Word A		W38	Loop 2 Control Word A	
W19	Loop 1 Control Word B		W39	Loop 2 Control Word B	
W20	Input Filter Time Constant 1	TA1	W40	Input Filter Time Constant 2	TA2
W21	Maximum Negative Error 1	EMN1	W41	Maximum Negative Error 2	EMN2
W22	Maximum Positive Error 1	EMP1	W42	Maximum Positive Error 2	EMP2
W23	Dead Band 1	DB1	W43	Dead Ban 2	DB2
W24	Integral Gain 1	K_I1	W44	Integral Gain 2	K_I2
W25	Derivative Gain 1	K_D1	W45	Derivative Gain 2	K_D2
W26	Integral Term Limit 1	V_IMAX1	W46	Integral Term Limit 2	V_IMAX2
W27	Derivative Term Limit 1	V_DMAX1	W47	Derivative Term Limit 2	V_DMAX2
W28	Minimum Output Limit 1	VMIN1	W48	Minimum Output Limit 2	VMIN2
W29	Maximum Output Limit 1	VMAX1	W49	Maximum Output Limit 2	VMAX2
W30	Loop 1 Expanded Control Word		W50	Loop 2 Expanded Control Word	
W31	Minimum Scaling Value 1	SMIN1	W51	Minimum Scaling Value 2	SMIN2
W32	Maximum Scaling Value 1	SMAX1	W52	Maximum Scaling Value 2	SMAX2
W33	Feedforward Offset 1	FFO1	W53	Feedforward Offset 2	FFO2
W34	Feedforward Gain 1	K_F1	W54	Feedforward Gain 2	K_F2
W35	Lead Time Constant 1	TB1	W55	Lead Time Constant 2	TB2
W36	Lag Time Constant 1	TC1	W56	Lag Time Constant 2	TC2

Note: If you change a loop 1 or loop 2 parameter, you must initiate a load/entry sequence.

Algorithm Flow Chart

The algorithm flow chart shows the selectable features of the PID module's control algorithms and indicates how selected features effect the entire algorithm.

The algorithm flow chart can be used as a road map when programming the PID module. Begin at the analog input. Select the needed features. Record their word and bit values on copies of the worksheet found in appendix A. When all needed features have been selected and the flow chart has been followed to completion, the selections can be entered into appropriate files in the PC processor. Data entry can be done after data table addresses have been assigned to the data block and the ladder diagram program has been entered into memory.

Prior to following the flow chart, there are five decisions concerning module features which must be made. These decisions and their corresponding control bits are not on the chart.

- 1-loop or 2-loop operation, W01 B15
- standard or expanded features, W01 B14
- 4-digit BCD or 12-bit binary data format for most analog terms, W01 B12
- 4-digit BCD or 12-bit binary data format for the set point, W01 B11
- soft fault response for each loop W38(W59) B15,14,13

The algorithm flow chart is shown in Figure 3.15. Sheet 1 shows, callouts, abbreviations, and how to interpret the flow chart. See Appendix E for an enlarged fold-out of the flow chart.

Block Transfer Programming

This section describes how the PID module is programmed. It also describes how the status of the PID module can be continuously read by the PC processor without performing read block transfers. Programming techniques and strategies are explained in this section. Example program/applications are presented in appendicies B and C. The programming explanations pertain to the PLC-2/30 processor. Programs can be modified for other processors capable of block transfer (refer to chapter 1).

Figure 3.15
Algorithm Flow Chart (3 sheets)

WORD / BIT CALLOUTS

SMIN	ABBREVIATION FOR MINIMUM SCALING VALUE
±9999	RANGE OF VALUES
W31 (W51)	PID MODULE WORD NUMBER. LOOP 1 (LOOP 2)
W19 B06	BIT NUMBER. (LOOP 2 NUMBERS ARE IN PARENTHESIS.)
M	PREFIX M MEANS MULTIPLER BIT(S).
S	PREFIX S MEANS SIGN BIT.
B/B	PREFIX B/B REFERS TO BCD/BINARY FORMAT BIT.
NO	LOGIC STATE 0
YES	LOGIC STATE 1

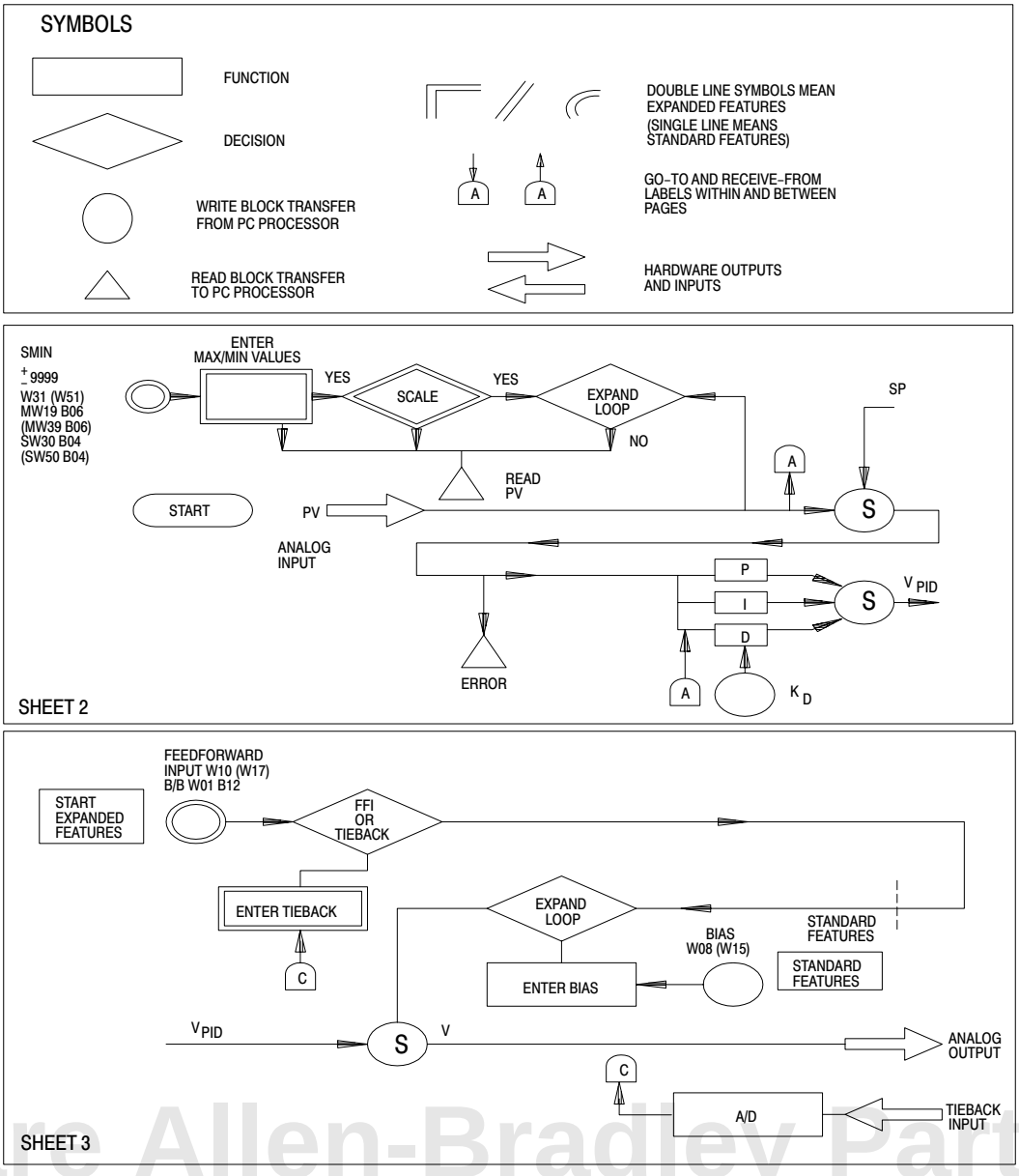
LEGEND SHEET

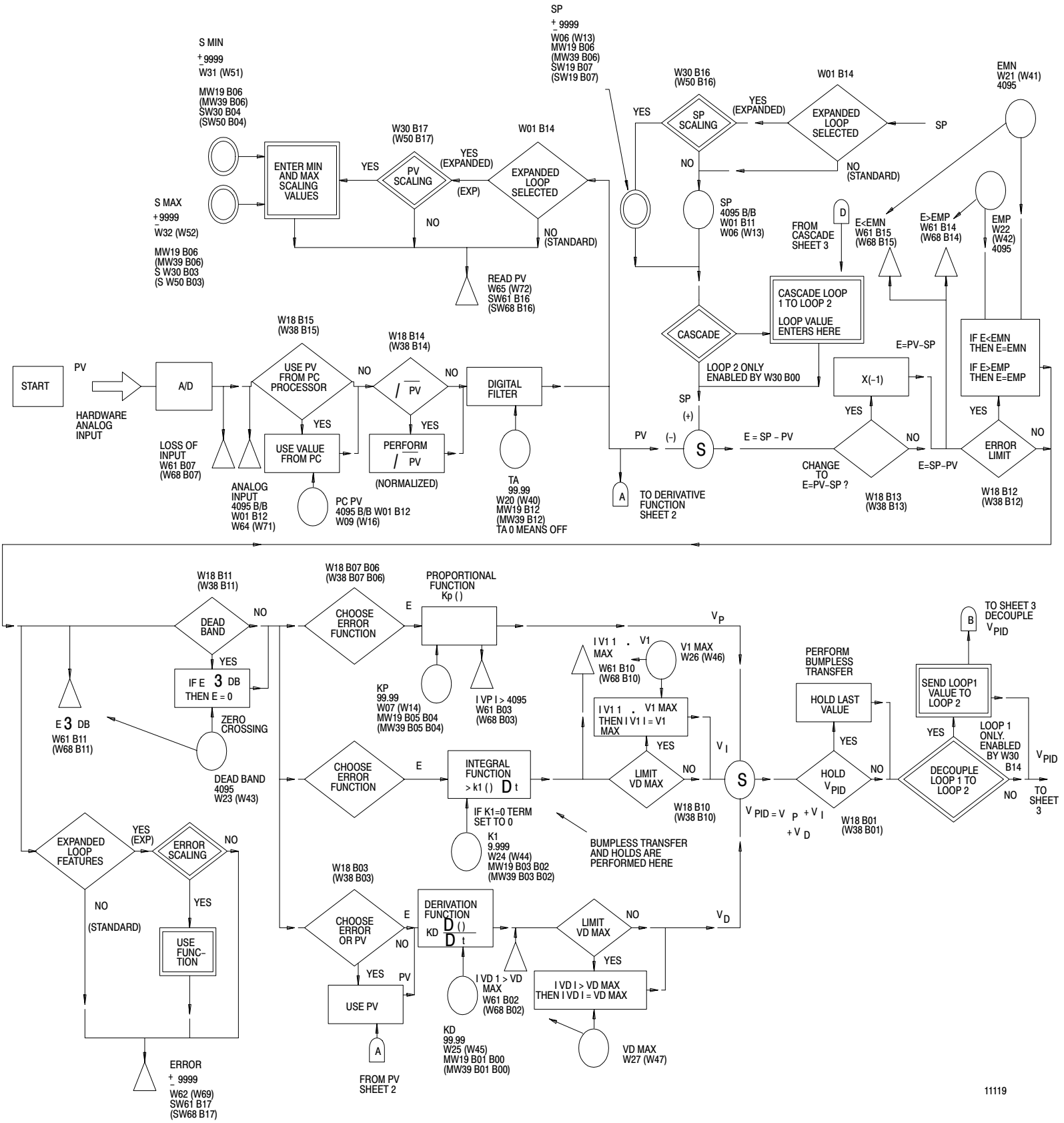
THE ALGORITHM FLOW CHART CONSISTS OF TWO PAGES WHICH FOLLOW ON SHEETS 2 AND 3. THEY ARE SHOWN BELOW IN ABBREVIATED FORM TO PRESENT THE GENERAL SIGNAL FLOW AND TO DEFINE THE SYMBOLS AND CALLOUTS USED THROUGHOUT. THE BOX AT THE UPPER LEFT DESCRIBES THE WORD/BIT CALLOUTS. THE BOX JUST BELOW DEFINES THE SYMBOLS.

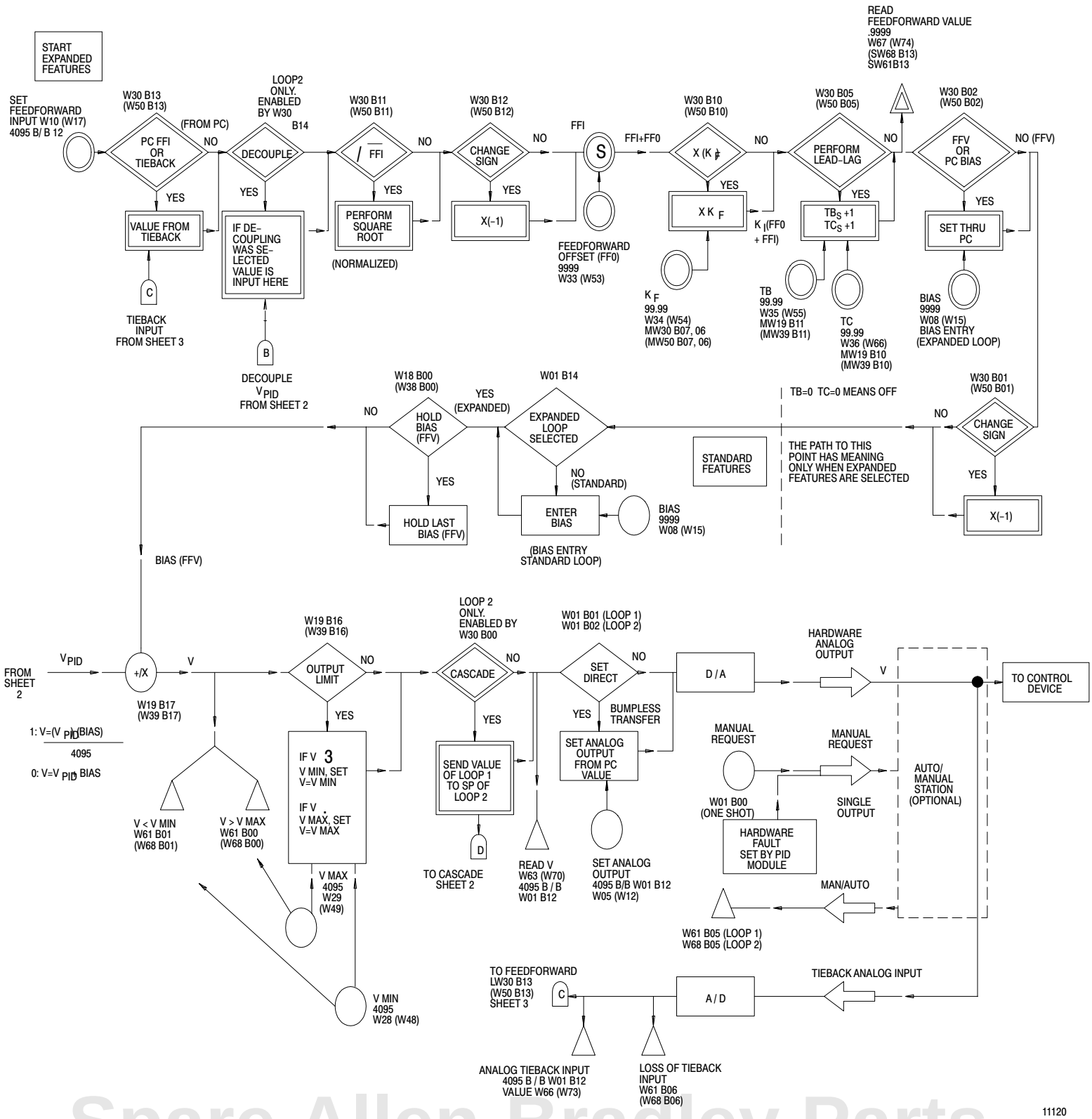
THERE ARE FIVE FEATURES NOT SHOWN ON THE CHART THAT SHOULD BE SELECTED BEFOREHAND:

1. ONE OR TWO LOOP OPERATION W01 B15
2. STANDARD OR EXPANDED FEATURES W01 B14
3. FOUR-DIGIT BCD OR 12-BIT BINARY FORMAT FOR SETPOINT, W01 B11
4. FOUR-DIGIT BCD OR 12-BIT BINARY FORMAT FOR ANALOG VALUES, W01 B12
5. SOFT FAULT RESPONSE FOR EACH LOOP, W39 (W59) B15, B14, B13

THE ALGORITHM FLOW CHART CAN BE USED AS A ROAD MAP WHEN PROGRAMMING. BEGIN AT THE ANALOG INPUT AND FOLLOW THE CHART TO DETERMINE WHICH FEATURES SHOULD BE IMPLEMENTED.




S MIN
±9999
W31 (W51)
MW19 B06
(MW39 B06)
SW30 B04
(SW50 B04)
S MAX
±9999
W32 (W52)
MW19 B06
(MW39 B06)
S W30 B03
(S W50 B03)
ENTER MIN AND MAX SCALING VALUES
W30 B17
(W50 B17)
PV SCALING
YES
YES (EXPANDED)
(EXP)
W01 B14
EXPANDED LOOP SELECTED
NO
NO (STANDARD)
READ PV
W65 (W72)
SW61 B16
(SW68 B16)
SP
±9999
W06 (W13)
MW19 B06
(MW39 B06)
SW19 B07
(SW19 B07)
W30 B16
(W50 B16)
SP SCALING
YES (EXPANDED)
EXPANDED LOOP SELECTED
SP
NO (STANDARD)
EMN
W21 (W41)
4095
SP
4095 B/B
W01 B11
W06 (W13)
FROM CASCADE SHEET 3
D
E<EMN
W61 B15
(W68 B15)
E>EMP
W61 B14
(W68 B14)
EMP
W22
(W42)
4095
CASCADE
CASCADE LOOP 1 TO LOOP 2
LOOP VALUE ENTERS HERE
LOOP 2 ONLY ENABLED BY W30 B00
E=PV–SP
X(–1)
IF E<EMN THEN E=EMN
IF E>EMP THEN E=EMP
START
PV
HARDWARE ANALOG INPUT
A/D
W18 B15
(W38 B15)
USE PV FROM PC PROCESSOR
W18 B14
(W38 B14)
1/PV
DIGITAL FILTER
LOSS OF INPUT
W61 B07
(W68 B07)
USE VALUE FROM PC
PERFORM 1/PV
(NORMALIZED)
ANALOG INPUT
4095 B/B
W01 B12
W64 (W71)
PC PV
4095 B/B W01 B12
W09 (W16)
TA
99.99
W20 (W40)
MW19 B12
(MW39 B12)
TA 0 MEANS OFF
A
TO DERIVATIVE FUNCTION SHEET 2
SP
(+)
PV
(–)
S
E = SP – PV
CHANGE TO E=PV–SP ?
E=SP–PV
ERROR LIMIT
W18 B13
(W38 B13)
W18 B12
(W38 B12)
W18 B11
(W38 B11)
DEAD BAND
E 3 DB
W61 B11
(W68 B11)
IF E 3 DB THEN E = 0
ZERO CROSSING
DEAD BAND
4095
W23 (W43)
W18 B07 B06
(W38 B07 B06)
CHOOSE ERROR FUNCTION
PROPORTIONAL FUNCTION
Kp ( )
E
KP
99.99
W07 (W14)
MW19 B05 B04
(MW39 B05 B04)
I VP I > 4095
W61 B03
(W68 B03)
VP
I V1 1 MAX
V1
V1 MAX
W26 (W46)
W61 B10
(W68 B10)
I V1 1 THEN I V1 I = V1 MAX
V1 MAX
LIMIT VD MAX
W18 B10
(W38 B10)
VI
PERFORM BUMPLESS TRANSFER
HOLD LAST VALUE
HOLD VPID
VPID = VP + VI + VD
W18 B01
(W38 B01)
TO SHEET 3
DECOUPLE VPID
B
SEND LOOP1 VALUE TO LOOP 2
LOOP 1 ONLY. ENABLED BY W30 B14
DECOUPLE LOOP 1 TO LOOP 2
VPID
TO SHEET 3
CHOOSE ERROR FUNCTION
E
INTEGRAL FUNCTION
> k1 ( ) D t
IF K1=0 TERM SET TO 0
K1
9.999
W24 (W44)
MW19 B03 B02
(MW39 B03 B02)
BUMPLESS TRANSFER AND HOLDS ARE PERFORMED HERE
EXPANDED LOOP FEATURES
YES (EXP)
ERROR SCALING
NO
YES
NO (STANDARD)
USE FUNC-TION
ERROR
±9999
W62 (W69)
SW61 B17
(SW68 B17)
W18 B03
(W38 B03)
CHOOSE ERROR OR PV
E
DERIVATION FUNCTION
KD D ( ) / D t
LIMIT VD MAX
VD
USE PV
PV
I VD 1 > VD MAX
W61 B02
(W68 B02)
I VD I > VD MAX THEN I VD I = VD MAX
KD
99.99
W25 (W45)
MW19 B01 B00
(MW39 B01 B00)
VD MAX
W27 (W47)
A
FROM PV SHEET 2
11119



Block Transfer Instruction Overview

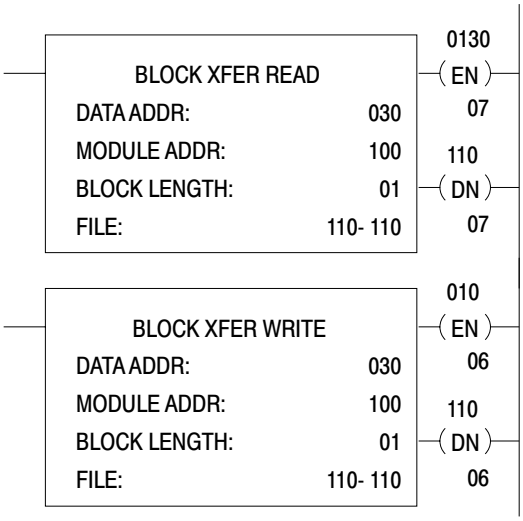
All programming data for the PID module must be contained in files residing in the PC processor's data table. The files are block transferred to the PID module where they are stored and used to perform PID control. Figure 3.16 and Figure 3.17 present a brief summary of block format block transfer instructions and data table locations.

NOTE: For PLC-2 family processors, the address of the file to be transferred in the address of the first word in the file. The file address is stored in BCD in a storage word located 100 8 above the instruction's data address. The number of words transferred must vary according to the number of words in any of the files. When the block length is set to the default value, the PID module will control the block length for each transfer. Otherwise, if a program is written that allows unequal block length other than default to be enabled in the same scan, incomplete data could be transferred.

Figure 3.16
Block Format Block Transfer Instructions

A block transfer instruction is programmed in the ladder diagram by deptressing the [BLOCK XFER] key followed by [1] (for a READ) or [0] (for a WRITE). The appropriate read or write block, as shown below will appear on the industrial terminal screen.

Numbers shown are default values. Numbers in shaded areas must be replaced by user-entered values. The number of default address digits initially displayed, 3, 4, or 5 will depend on the size of the data table. Initially displayed default values are governed by the I/O rack configuration.



Data Address	: First, possible address in accumulated value area of data table.
Module Address	: Rack, module group, and slot number.
Block Length	: Number of words to be transferred. (00 can be entered for default value or for 64 words)
File	: Address of first word in the file. Storage location is 100 8 above the data address.
Enable Bit (EN)	: Automatically entered from the module address. Set on when rung containing the instruction is true.
Done Bit (DN)	: Automatically entered from the module address. Remains on for 1 scan following successful transfer.

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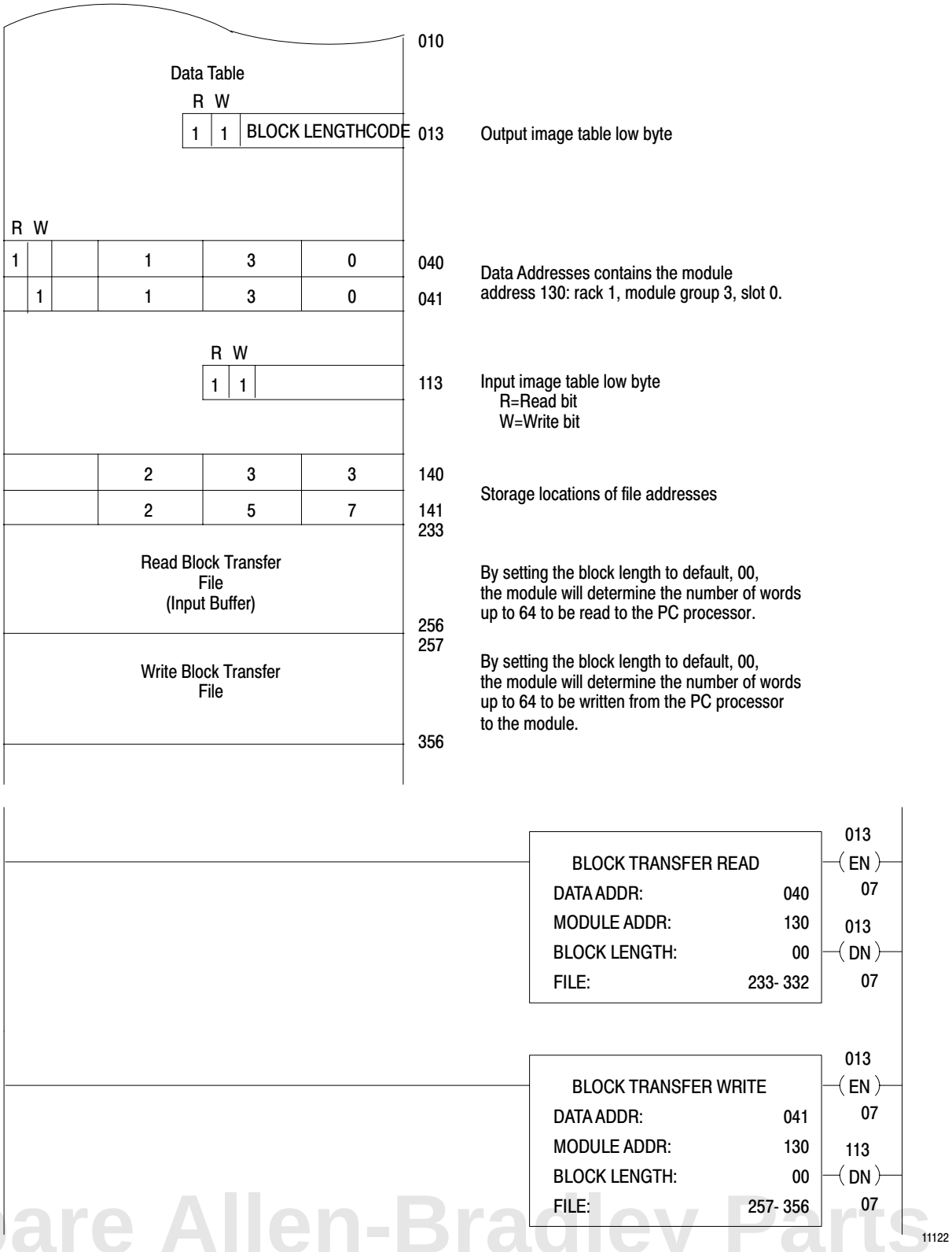
Figure 3.17
Example Data Table Locations for Bidirectional Block Transfer



Those unfamiliar with block transfer programming techniques should read the explanation found in the programming and Operation Manual for the PC processor being used. It is important to under block transfer concepts before reading this section.

Block Transfer Sequencing

The PID module is designed to sequence the multiple block transfers required to program the module and actively communicate with the PC processor. The PID module can prompt a block transfer sequence by sending to the PC processor the data table address of the first word in the file to be transferred next in the sequence. A rung in the ladder diagram program is required to manipulate the file address in the write block transfer instruction.

The data table address of each of the three data blocks is written to the PID module in the dynamic block transfer. One word defines the starting address of each block:

W03 dynamic block start address
W04 loop 1 block start address
W11 loop 2 block start address

The PID module returns to the PC processor the data table address (next block start address) of the next block to be transferred. The address is the value in word W59 in the status block. Two rungs are required to perform the prompting (Figure 3.18). During normal operation rung A gets the value returned by the PID module in word W59 and puts it in the file address storage word of the write block transfer instruction. The user program automatically performs the next block transfer required in the sequence determined in this manner by the PID module.

Rung B is active only at power-up. If the module is in the power-up mode and is unprogrammed, it cannot automatically prompt a block transfer. Instead, the PID module returns the power-up bit W58 B13 = 1 to a data table storage bit such as 350/13. The power-up bit controls rung B. At power-up only, rung B forces the write block transfer instruction to transfer the dynamic block. The dynamic block contains the block start address for each of the three write blocks. After the PID module receives this transfer, it can control the sequencing with rung A.

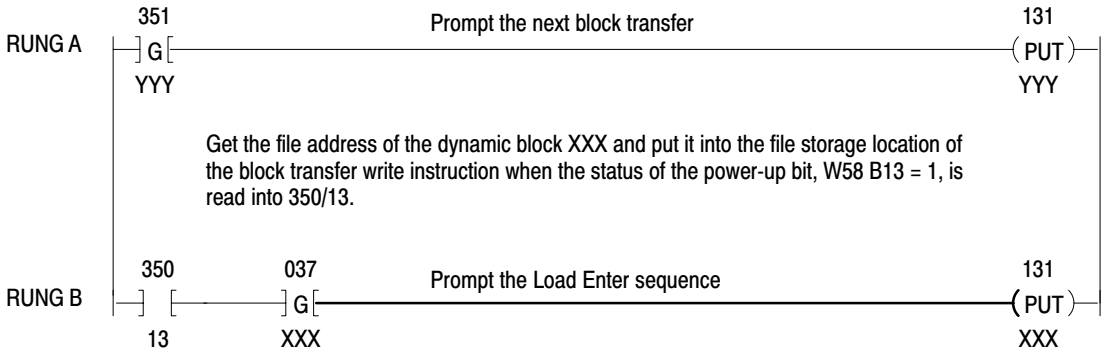
Block transfer sequencing must be programmed for each of the following:

- dynamic/status toggle sequence
- power-up load/enter sequence
- load/enter sequence

Figure 3.18
Programming the Load/Enter Sequence

The next block start address YYY in word W59 is read into data table word 351_8 when the status block is transferred to the PC processor.

Get the file address of the next block to be transferred YYY, and put it into the file storage location of the block transfer write instruction.



NOTE: Words 037, 350 and 351 can be any data table storage words

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The term dynamic/status toggle sequence describes the operating mode of alternating read and write block transfers. The sequence allows dynamic block data to be changed without changing the loop constants. The status block is read to prompt the next write block transfer and to report status, alarm and diagnostic information. The dynamic block is transferred to change any of the dynamic block values such as the set analog output value, set point, proportional gain, and bias. Block transfers can occur in only one direction at a time. Toggling implies that a read block transfer must be completed before a write block transfer is requested.

There are a few bits which establish the module configuration which also cannot be changed in this sequence. There are denoted by the symbol (LE). If changes to these bits are transferred to the module, they will be ignored until a load/enter sequence is complete. These bits are W01 B15,

B14, B12, B11 defined in section titled Dynamic Block: Words W01-W17.

Status Monitor Byte

The status monitor byte, SMB, allows the status of the PID module to be reported without performing a read block transfer. By using the status monitor byte it is possible to examine the general status of the PID module. Whenever a block transfer is not being requested, the status monitor byte data is transferred to the input image area of the PC data table designated by the rack number, module group number, and lower slot number of the PID module.

Bits B04-B00 are used to report module status. Bits B07-B05 are used to precondition the status bits to ensure their validity.

NOTE: The user program should monitor the preconditioned bits B04-B00 to enable a read block transfer of the status block whenever an SMB status bit goes high.

The SMB bits are defined below and are illustrated in Figure 3.19. An example of preconditioning is illustrated in Figure 3.20.

SMB B07 **Precondition.** Set to 1 indicates the byte is invalid. Reset to 0 when the byte is valid.

SMB B06 **Precondition.** Set to 1 indicates the byte is invalid. Reset to 0 when the byte is valid.

SMB B05 **Precondition**. Set to 1 indicates the byte is valid. Reset to 0 when the byte is invalid.

SMB B04 **Alarm.** Set to 1 when an alarm condition exists as reported by the loop status word W61(W68). Reset to 0 indicates no alarm condition have been detected. The alarm conditions and corresponding status bits which set SMB B04 =1 are listed in table 3.K.

Also, SMB B04 will be set to 1 if the dynamic block error bit W58 B15 or the loop block error bit W58 B14 is set to 1. Then the loop time/diagnostic bit W01 B07 should be set high (concurrently) so that the diagnostic data in word W60 can be reported.

SMB B03 **Power-up.** Set to 1 if the module is in power-up mode. Reset to 0 after the first valid dynamic block transfer. SMB B03 mirrors the status of W58 B13.

SMB B02 **Loss of Input.** Set to 1 when any one of the four inputs (analog input 1 or 2, tieback input 1 or 2) is absent. Reset to 0 when the input signal is within the standard range of +1 to +5VDC or +4 to +20mA.

SMB B01 **Loss of +15VDC.** Set to 1 for loss of +15VDC power. Reset to 0 indicates power is present. SMB B01 mirrors the status of W58 B11.

SMB B00 **Soft Fault Mode.** Set to 1 in soft fault mode. Reset to 0 when in normal operating mode. SMB B00 mirrors the status of W58 B10.

Figure 3.19
Status Monitor Byte

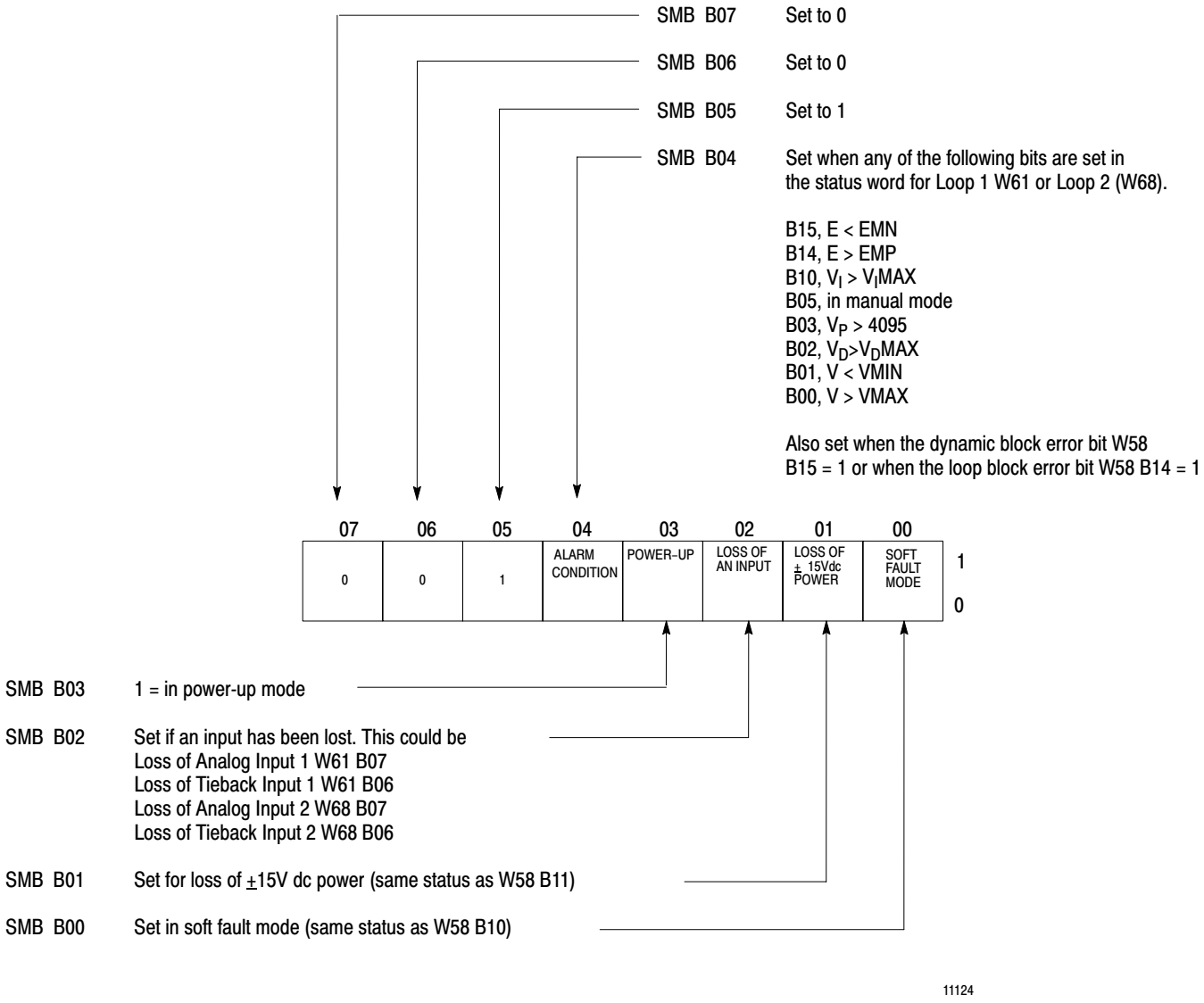

Figure 3.20
Status Monitor Byte Preconditioning

The condition of bits B07, B06, B05 must be examined to determine if the other five bits are valid. B07 and B06 must be 0. B05 must be 1.

The rungs below show one technique for preconditioning:

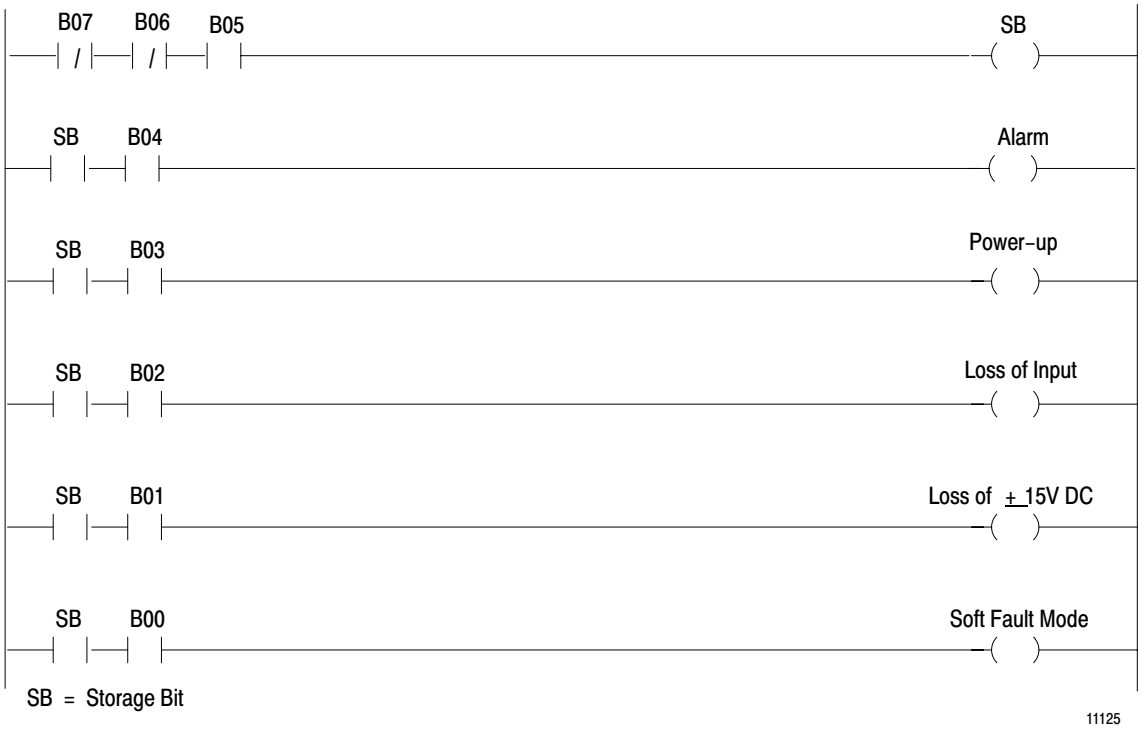

Table 3.K
Loop Block Alarm Conditions

Condition	Alarm Bit
E<EMN	W61(W58)B15
E>EMP	W61(W68)B14
V_I>V_IMAX	W62(W58)B10
In Manual Mode	W61(W68)B05
VP>4095	W61(W68)B03
V_D>V_DMAX	W61(W68)B02
V<VMIN	W61(W68)B01
V>VMAX	W61(W68)B00
Dynamic block error	W58 B15
Loop block error	W58 B14

Power-Up Load/Enter Sequence

A power-up load/enter sequence is required for initial power-up or after the module resets itself from the restoration of +5VDC power. This sequence is a series of block transfers that begins with the module clearing its memory of all previously stored data.

There are two control bits and four status bits used in the power-up load/enter sequence (Table 3.L).

The power-up load/enter sequence is outlined below and illustrated in Figure 3.21. Refer to Block Transfer Sequencing, section titled Block Transfer Sequencing.

Transfer 1 - The processor reads the status block in the first block transfer. Word W58 will be returned with the power-up bit W58 B13 set to 1 indicating that the PID module has just been powered-up and has not yet been initialized.

The RUN LED on the module will be flashing. Other LEDs will be off. This indicates the module has power but has not yet been programmed.

Transfer 2 - The processor writes the dynamic block data to the module in this block transfer. Load bit W01 B06 is set to 1.

Transfer 3 - The read block transfer will prompt the loading of loop 1 constants by returning the loop 1 block start address W04 in word W59. The status block will contain the power-up bit W58 B13 reset 0.

Transfer 4 - The write block transfer must contain the loop 1 constants. If incorrect values are transferred during initialization, the load sequence is held at this point until values are corrected. The load/enter sequence then resumes.

Transfer 5 - The read block transfer will prompt the loading of loop 2 constants by returning the loop 2 block start address W11 in the word W59.

Transfer 6 - The write block transfer must contain the loop 2 constants.

Transfer 7 - The read block transfer will prompt the dynamic block by returning the dynamic block start address W03 in word W59. This transfer will contain the ready bit W58 B12 set to 1.

Transfer 8 - The write block transfer must have the enter bit W01 B03 set to 1. This bit must be set during the initial power-up sequence.

Transfer 9 - The read block transfer will have ready bit W58 B12 reset to 0 and will have the load/enter complete bit W61 B12 and the power-up complete bit W61 B04 set to 1. This indicates that the PID module has been programmed and that no errors were detected in the dynamic block or loop blocks.

After the power-up load/enter sequence, the PID module automatically sets itself for the next transfer of the dynamic block. Program logic can immediately initiate the dynamic/status toggle sequence, or it can halt communication until prompted by a timer and/or SMB error bit.

Table 3.L
Load/Enter Bits

Bit Name	Bit Number
load enter	W01 B06 W01 B03
power-up ready	W58 B13 W58 B12
load/enter complete power-up complete	W61 B12 W61 B04

Figure 3.21
Power-Up Load/Enter Sequence

Command		Block Transfers	Status			
Load Bit W01 B06	Enter Bit W01 B03	read / write	Power-up Bit W58 B13	Ready Bit W58 B12	Load Enter Complete Bit W61 B12	Power-up Bit W61 B04
1	0	1st SB → PROCESSOR; 2nd DB ← PID MODULE	1	0	0	0
1	0	3rd SB → PROCESSOR; 4th LP1 ← PID MODULE	0	0	0	0
1	0	5th SB → PROCESSOR; 6th LP2 ← PID MODULE	0	0	0	0
0	1	7th SB → PROCESSOR; 8th DB ← PID MODULE	0	1	0	0
0	0	9th SB → PROCESSOR; DB ← PID MODULE; SB → PROCESSOR	0	0	1	1
0	0	DB ← PID MODULE; SB → PROCESSOR	0	0	1	1

SB = Status Block, DB = Dynamic Block, LP1 and LP2 = Loop 1 and Loop 2 Parameter Blocks

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Load/Enter Sequence

The load/enter sequence permits selected word and bit data to be transferred to the PID module in a manner that protects the data from accidental change which could adversely affect the controlled process. The load/enter sequence is used during normal operation when loop 1 and loop 2 constants and bits B15, B14, B12, B11 in the master control word W01 must be changed.

The load/enter sequence is similar to the power-up load/enter sequence. However, the power-up bit is not examined, and the enter bit can be delayed. During initialization, the exact sequence described in section titled Power-Up Load/Enter Sequence must be followed. Thereafter, it is possible to transfer loop constants in a load/enter sequence before they are needed for a change to the control process. Loop constants can be stored indefinitely in the PID module's buffer until the enter bit is transferred, completing the load/enter sequence.

NOTE: Dynamic block data can be transferred to the PID module when needed by a write block transfer. Or, dynamic block data can be continuously transferred to the PID module in the dynamic/status toggle sequence. Dynamic block values are implemented immediately upon transfer. In contrast, loop 1 and loop 2 constants require a load/enter sequence and are buffered in the PID module until the enter bit is set.

The load/enter sequence is shown in Figure 3.22 and is similar to the power-up load/enter sequence outlined in section titled Power-Up Load/Enter Sequence.

Transfer 1 - The load/enter sequence is initiated by writing the dynamic block data to the PID module. The load bit W01 B06 is set to 1. The values transferred in this block are used immediately by the PID module. The bits W01 B15, B14, B12, B11 which can redefine the module configuration are not acted upon until the enter portion of the load/enter sequence is performed.

If an error is detected in the dynamic block data, the new data will be ignored. The PID module will set the dynamic block error bit W58 B15 high and will continue PID control based on previous dynamic block data.

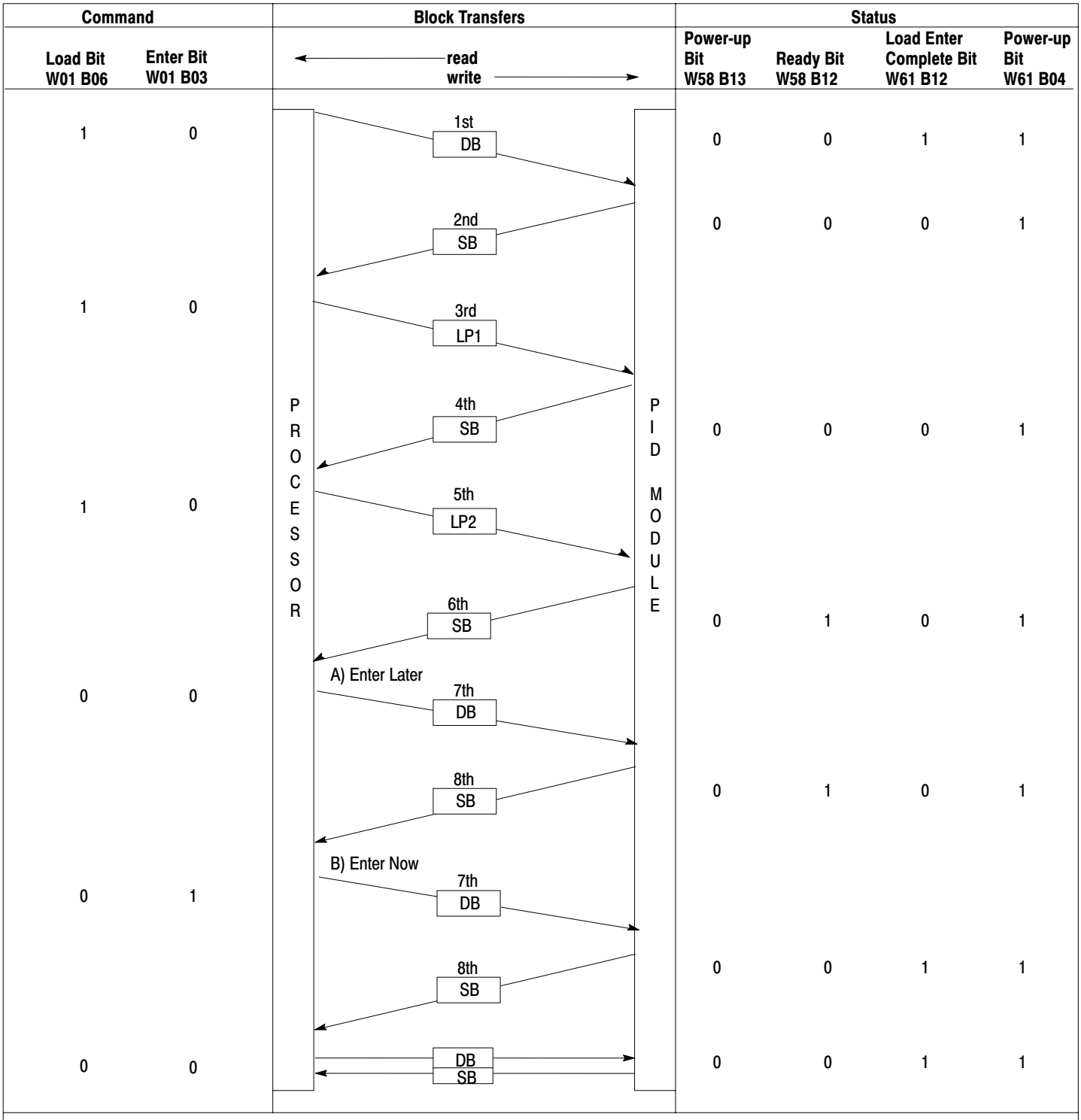
Transfer 2 - The processor read the status block to determine the next block start address.

Transfer 3 - The processor writes the loop 2 block to the PID module where it is stored in a buffer.

If an error is detected in loop 1 block data, the new data will be ignored. The sequence will toggle between transfer 2 and 3 until the error is corrected. The module will set the loop block error bit W58 B14 high and will continue PID control based on previous loop block data.

Transfer 4 - The processor reads the status block to determine the next block start address.

Figure 3.22
Load/Enter Sequence



SB = Status Block, DB = Dynamic Block, LP1 and LP2 = Loop 1 and Loop 2 Parameter Blocks

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Transfer 5 - The processor writes the loop 2 block to the PID module where it is stored in a buffer.

If an error is detected in loop 2 block data, the new data will be ignored. The sequence will toggle between transfers 4 and 5 until the error is corrected. The module will set the loop block error bit W58 B14 high and will continue PID control based on the previous loop block data.

Transfer 6 - The processor reads the status block to determine the next block start address. The block contains ready bit W58 B12 set to 1 which indicates the new data was valid.

At this point in the sequence, one of two paths may be taken. The enter portion of the load/enter sequence can be performed immediately or the data can be maintained in the buffer until activated.

A) Enter later:

Transfer 7 - The processor writes the dynamic block to the PID module. The load bit W01 B06 is reset to 0 preventing a new load/enter sequence from starting. Loop 1 and loop 2 constants remain stored in the module buffer because the enter bit is not set.

Transfer 7 repeats as long as the enter bit remains reset.

New dynamic values to be used with the stored loop constants should be transferred until the enter bit is transferred.

Transfer 8 - The read transfer of the status block will prompt the write transfer of dynamic block. The ready bit W58 B12 information was valid and the PID module is waiting for the enter command W01 B03 set to 1.

The enter bit must be set to 1 for the new loop constants to become active as explained in part b.

B) Enter now:

Transfer 7 - The processor writes the dynamic block to the PID module with enter bit W01 B03 set to 1. The PID module will begin control based on the data received in the dynamic block. The loop 1 and loop 2 constants which were received and buffered become active.

Transfer 8 - The processor reads the status block with the ready bit W58 B12 reset to 0 and the load/enter complete bit W61 B13 set to 0. This indicates that the buffered loop constants are being used to perform PID control.

When the load/enter sequence is complete, The PID module automatically sets itself for a dynamic block transfer or dynamic/status toggle sequence initiated by using program.

NOTE: Loop 1 and loop 2 constants can be transferred to the PID module and stored for future use. Later, when the enter bit is transferred, any change in the dynamic block that are required for use with the new loop constants should be transferred when the enter bit W01 B03 is set to 1. If transferred before the enter bit, the dynamic block changes will be enabled without the corresponding changes to the loop constants. Dynamic block values except for bits W01 B15, B14, B12, B11 are implemented when transferred. The four bits and the loop constants require a load/enter sequence to be completed before they can be implemented.

Programming Considerations

The general concepts required for programming the PID module have been explained in the previous sections. The following sections provide additional information for applying these concepts in specific situations.

Section titled Load/Enter Sequence for Loop 1 operation explains the changes which are required if only loop 1 is programmed.

Section titled Periodic Block Transfer explains the technique of performing block transfers initiated by the status monitor byte or by a block transfer watchdog timer.

Section titled Block Transfer Timing explains module block transfer timing and system scan timing.

Load/Enter Sequence for One-Loop Operation

All references to the various block transfer sequences so far have assumed 2-loop operation. when the PID module is selected for loop 1 only operation by setting W01 B15 to 1, the initial power-up load/enter sequence is shortened. After loop 1 values are received (transfer 3 in Figure 3.22) the read transfer will not prompt loop 2 but will prompt the dynamic block instead. In effect, transfers 4 and 5 are skipped and the

PID module goes directly to transfer 6 which prompts the dynamic block. Review section title Load/Enter Sequence if necessary.

The prompting is controlled by the PID module. Note that the program in appendix B is selected for loop 1, only. To program two loops, the ladder diagram program would not change. Only the bit selection is changed to select the 2-loop feature. Loop 2 values would have to be entered into the appropriate file.

Periodic Block Transfer

When the PC processor is communicating with many block transfer modules, it may be desirable to reduce the number of continuous block transfers in order to reduce the system scan time. This can be done by performing block transfers periodically or only when they are required. The technique may not apply to all applications.

The technique is based on the capability of the status monitor byte to report the general status of the PID module without a read block transfer. No block transfers are performed until necessary. If a fault is detected and indicated in the status monitor byte, the dynamic/status toggle sequence is enabled by program logic until the problem can be located and corrected.

The status monitor byte should never by used alone to determine module status. Periodic read block transfers should be initiated to verify proper operation. A fee-running timer should be added to the ladder diagram program to request a read block transfer at timed intervals. In the event of a PID module or communications failure, the status monitor byte will not be updated to show a fault. However, the faulted module will not perform a block transfer. The watchdog timer for the read block transfer will time out to indicate that the PID module is no longer communicating with the PC processor. This technique is used in the program in appendix C.

Block Transfer Timing

There are two areas of block transfer timing: module timing and system timing. Module timing refers to the time required to process the transferred data, perform the PID algorithm and prepare for the next block transfer. This is typically 100 msec (110msec max.) regardless of the number of words transferred to the PID module. Once a block transfer is completed, another transfer will not be permitted until the next loop update is complete. Module timing is also the loop update time referred

to in section titled Status Block: W57-W74 word W60 Loop Time/Diagnostic. Refer to Figure 3.11.

System timing refers to the time required to scan the ladder diagram program and to communicate between PC processor and PID module. System timing depends on the kind of PC processor used, the number of words transferred, the number of I/O racks in the system, the number of enabled block transfer instructions in the ladder diagram program during any program scan and the length of user program.

PLC-2/30 REMOTE SYSTEM

The system scan time for a remote PLC-2/30 system must include the processor scan time, the processor I/O scan time (between processor and remote distribution panel), and the remote distribution panel I/O scan time. Assume that for a remote system, the Remote Distribution Panel (cat. no. 1771-SD) can process only one block transfer operation per processor I/O scan.

The procedure for calculating the worst case time for a read or write block transfer under normal operating conditions can be done in three steps.

1. Calculate the system values that are determined by the system configuration.

- Program Scan PS = (5msec/lK words) x (number of program words)
- Processor I/O Scan PI0 = (0.5msec/rack number) x (assigned rack numbers)
- Remote Distribution I/O Scan RI0 = (7msec/chassis) x (number of chassis)
- Number of Words Transferred W = 18 for a read or write. (Although this number can be 17, 18 or 19, 18 has been chosen for simplicity.)

2. Calculate the block transfer time TW for the write or read operation which are essentially the same. This time includes system timing and module timing if greater than 100msec.

$$TW = PS + PI0 + 2\ RI0 + .5W + 9 \quad \text{(equation 1)}$$

NOTE: If the calculated time TW is less than 100msec. an alternative equation must be used to calculate the time for a single write or read operation.

TW' = 100 + RI0 + .5W + 9 (equation 2 for when TW<100msec)

The equations for TW or TW' can be used to calculate the time for a single write or read operation when no other block transfer modules are in the system.

The worst case block transfer time TW or TW' starts when the block transfer instruction is enabled in the ladder diagram program and ends when the module has received the transfer and the PC processor has received the done bit and is ready for the next transfer. It includes system time and module time. However, when block transfer instructions are enabled for other block transfer modules in the system, it is possible that all other modules could be given priority to perform one block transfer ahead of the subject module. This queuing effect must be considered when calculating the worst case time T Q, for a single read or write operation as follows:

$$T_Q = TW + T_{BT1} + T_{BT2} + T_{BT3} + ... \qquad \text{(equation 3)}$$

NOTE: The time for one block transfer operation, such as T BT1, of another block transfer module can be calculated using the following equation.

$$T_{BT} = PS + PI0 + 2\ RI0 + .5W + 9 \qquad \text{(equation 4)}$$

3. Calculate the time required for a load/enter sequence.

When calculating the worst case time for an entire load/enter block transfer sequence, multiply the individual block transfer times TW by the number of block transfer in the sequence. This will give an estimated times for a single PID module in a remote system where no other block transfer modules are present; or when the block transfer instructions of all other block transfer modules are not enabled during the load/enter sequence.

When there are other block transfer modules in the system performing a write or read operation during the load/enter sequence, the transfer times of these modules must be considered. For worst case, assume that all other block transfer modules are queued and have priority to perform one block transfer ahead of the PID module during each transfer of the load/enter sequence. The total time for the load/enter sequence will be

the number of transfers in the sequence multiplied by the sum of all possible block transfer times.

$$T_{LE} = (\text{\# transfers in the sequence}) \times (T_Q) \qquad \text{(equation 5)}$$

Example Problem 1

A PID module in a remote system controls two expanded loops. It is the only block transfer module in the remote system.

Processor = PLC -2/30
I/O = 2 remote chassis (two rack numbers)
Program = 1K words
Words transferred = 18

a. Calculate the time for a single read or write block transfer.

b. Calculate the time required for a load/enter sequence.

Solution, part a)

1. Calculate the system values
PS = Program Scan = (5msec/lK)(1K) = 5msec
PI0 = Processor I/O Scan = (0.5msec/rack number)x(2 rack numbers) = 1msec
RI0 = Remote I/O Scan = (7msec/chassis)x(2 chassis) = 14msec
W + Number of words transferred = 18 for a read or write

2. Calculate the time for a single read or write operation.
TW = PS + PI0 + 2 RI0 + .5W + 9
= 5 + 1 +2(14) + .5(18) + 9
= 52 msec

NOTE: This is less than 100 msec. Use the alternate formula for the transfer time.

TW' = 100 + RI0 + .5W + 9
= 100 + 14 _ 5.(18) +9
= 132msec

Solution, part b)

A normal load/enter sequence contains seven consecutive alternating read and write block transfers.

dynamic block (write)
status block (read)
loop 1 block (write)
status block (read)
loop 2 block (write)
status block (read)
dynamic block (write)

Using the value of TW' = 132msec for a single read or write operation from step 2, the total time for a normal load/enter sequence is:

T_{LE}= (7) x (TW')
= 7 x 132
= 924msec

Example Problem 2

A Pid module in a remote system controls two expanded loops. The remote system contains another block transfer module that transfers 64 words.

Processor = PLC-2/30
I/O = 6 remote chassis (six rack numbers)
Program = 8K words
Number of words transferred = 18 (PID)
Number of words transferred = 64 (other module)

a. Calculate the time for a single read or write block transfer.

b. Calculate the time required for a load/enter sequence when the other block transfer module is performing block transfers.

Solution , part a

1. Calculate the system values
PS = Program Scan - (5msec/lK)x(8K) = 40msec
PI0 = Processor I/O Scan = (0.5msec/rack number) x(6 rack numbers)=3msec
RI0 = Remote I/>O Scan = (7msec/chassis)x(6 chassis) = 42msec
W = Number of words transferred = 18 for a read or write (PID module)

2. Calculate the block transfer time for a single transfer.
TW = PS + PI0 + 2 RI0 + .5W +9
= 40 + 3 + 84 + .5(18) +9
= 145msec

Solution, part b
For the worst case calculation of a load/enter sequence, assume that the block transfer instruction for the other module will be enabled at the same time and will have priority during each transfer.

The time required for the other module to perform a 64 word block transfer is (from equation 4)

T_{BTI} = PS + PI0 + 2 RI0 + .5W + 9
= 40 + 3 + 84 + 32 + 9
=168msec

The time required for the PID module to perform a block transfer as calculated in solution, part a is TW = 145msec.
The total time for a single read or write operation when there is queueing due to other block transfer modules is (from equation 3).

T_Q = TW + T_{BTI}
T_Q = 145 + 168
T_Q = 313msec

The total time for the 7-transfer load/enter sequence is (from equation 5)

T_{LE} = (# transfers in the sequence x (T_Q from equation 3)
= 7(313)
= 2191msec
= 2.2 seconds

Expanded Features

The PID module can be user-configured to provide many types of closed loop control. The PID module can perform single element control, cascade, feedforward, cascade and feedforward, decouple (multi-loop, multi-variable) and PC processor interactive control. Other features such as scaling, digital filtering, and lead/lag can be selected to supplement the basic control function.

Expanded features of the module are described below.

Scaling

Scaling is the linear conversion of raw data to engineering units and vice versa, such as gallons/minute, degrees centigrade, and pounds/square inch. Unscaled data in the PID module has a range of 0 through 4095. The resolution of this data is 12 bit binary corresponding to 1 part in 4095. The resolution of scaled values is the same as the raw data, 1 part in 4095 regardless of the chosen scaling.

Scaling is an expanded loop feature which can be performed on the process variable, set point and/or error terms. Scaled process variable and error values can be read from the PID module and/or scaled set point values can be written to the PID module in scaled units by the PC processor. Each loop can perform scaling independent of the other.

The scaling feature is implemented by selecting expanded features by setting W01 B14; by setting bit B17 for the process variable, B16 for set point and/or B15 for error in word W30(W50); and by entering the minimum and maximum scaling values SMIN and SMAX. SMIN in word W32(W51) is the value corresponding to the bottom of the scale. SMAX in word W32(W52) is the top of the scale. When the minimum and maximum values are chosen and scaling is selected, the scaled values will be found in the following words.

- set point W06(W13)
- loop error W62(W69)
- process variable W65(W72)

Scaling Example 1

This example describes the scaling of flow transmitter data in loop 1. READ PV values are reported to the PC processor in word W65. Selected values with and without scaling are tabulated in table 3.M.

Values are read and displayed in engineering units of gallons/minute. The flow transmitter outputs a signal from +4 to +20mA. The range of the flow transmitter is 10 gallons/minute at +4mA and 70 gallons/minute at +20mA. A 10 gallons/minute rate is reported as 0000 when scaling is not used

Table 3.M
Scaling

Analog Signal	Actual Flow Rate	W65 READ PV1 Without Scaling	W65 READ PV1 With Scaling
+20mA	70 gallons/minute	4095	70
+16mA	55 gallons/minute	3072	55
+12mA	40 gallons/minute	2048	40
+ 8mA	25 gallons/minute	1024	25
+ 4mA	10 gallons/minute	0000	10
		1 part in 4096	gallons/minute
		no scaling	**scaling**
		W30 B17=0	W30 B17 = 1
			W30 B04, B03 = 0
			SMIN1 W31 = 10
			SMAX1 W32 = 70

Next assume that the process variable and the set point are scaled but the error term is not. SP1 is 40 gallons/minute. The flow rate at the PV1 input is 25 gallons/minute. The unscaled values are SP1 = 2048 and PV 1 = 1024. ERROR = SP - PV. Since ERROR1 is reported unscaled, the value will be 1024. If the error term had been scaled, the value of 15 would have been reported. This was obtained by subtracting the PV value from the SP value.

Scaling Example 2

In example 2, the lower limit of the process variable range SMIN is a negative number. Selected values of the scaled and unscaled process variable as read in word W65(W72) are listed in table 3.N. The current input varies from +4 to +20ma for a temperature range of -20^0C to $+60^0$C. The scale limits SMAX and SMIN are stored in words W32(W52) and

W32(W51), respectively. The negative sign of SMIN is set by W30(W50) B04 = 1.

Table 3.N
Scaling With Negative SMIN

Analog Signal	Actual Flow Rate	W65 READ PV1 Without Scaling	W65 READ PV1 With Scaling
+20mA	+60C	4095	60
+16mA	+40C	3072	40
+12mA	+20C	2048	20
+ 8mA	0C	1024	0
+ 4mA	-20°C	0000	20[1]
		no scaling	**scaling**
		W30 B17=0	W30 B17 = 1 SMIN W31 = 20 W30 B04 = 1[2] SMAX W32 = 60 W30 B03 = 0

[1] W6 B16 must be read to determine the signed of the scaled value in word W65. In this case, W61 B16=1 indicates a negative value.

[2] When the minimum scaling sign bit W30 B04=1, the minimum scaling value in W31 is negative.

Digital Filtering

Although not an expanded feature, digital filtering can be applied to analog input signals to reduce the effects of electrical noise. Digital filtering is done by a weighted moving average technique (Figure 3.23). The digital filter equation (Figure 3.24) uses the input filter time TA stored in word W20(W40).

Figure 3.23
Digital Filter

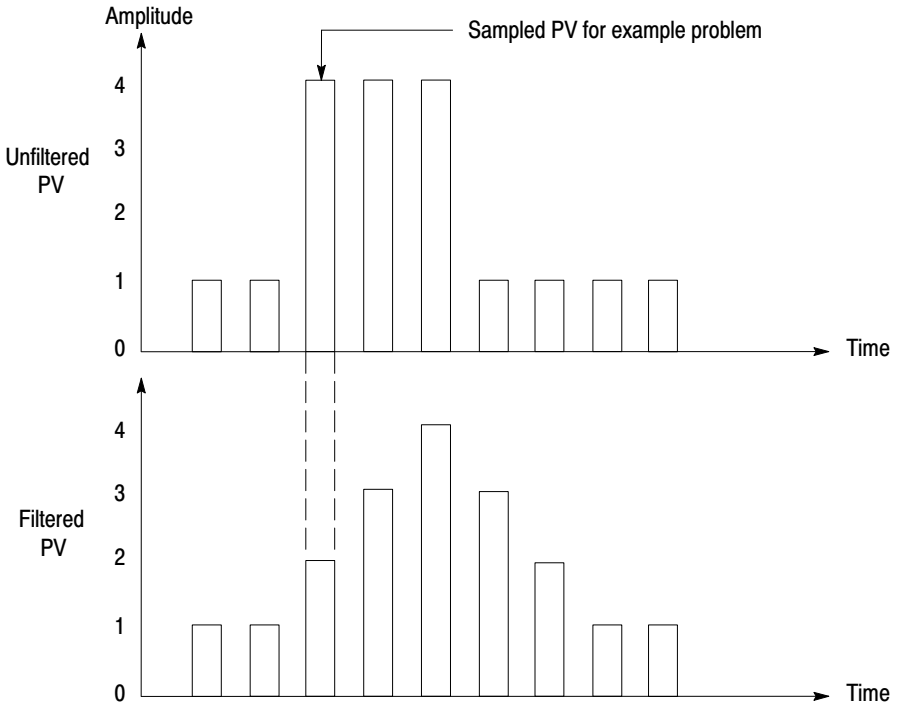

Figure 3.24
Digital Filter Equation

$$Y_n = Y_{n-1} + \frac{0.10}{TA}(X_n - Y_{n-1})$$

where

Y_n = present output, filtered PV
Y_{n-1} = previous output, filtered PV
0.10 = module loop update time
TA = digital filter time constant
X_n = present input, unfiltered PV

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For example, the sampling of PV values (Figure 3.23) shows a step change for three samples and then returns to the initial value. Using the digital filter equation (Figure 3.23) and a filter time constant of 0.3 seconds, calculate the filtered amplitude, Y_n, of the third sample.

Y_n-1 = 1.0V
TA = .33
X_n= 4.0

$$Y_n = 1.0 + \frac{010}{.33\ (4-1.0)}$$

$$=1.0 + .3(3)$$

$$=1.9$$

Lead/Lag Filter

Lead/lag filtering provides overcompensation or undercompensation of a feedforward input. The explanation of the lead/lag filter will be based on a step input.

With no filter, the step change is unaffected. With lead compensation, the initial step change is overcompensated and then settles out to the step change based on the value of the lead time constant TB. Lead compensation is shown as control above the step input value (Figure 3.25). With lag compensation, the initial step change is undercompensated and then settles out to the step change based on the value of the lag time constant TC. Lag compensation is shown as control below the step input value (Figure 3.26).

When values are entered for both lead and lag, the value with the larger magnitude will dominate the response. Thus 2/1 is a lead dominated response and l/2 is a lag dominated response. Lead/lag can be any ratio but the filter will limit the overcompensation (lead value) to eight times the step input value.

Also observe that the response time of a lead/lag filter having a given ratio will depend on the magnitute of the numerator and/or denominator. For example, a lead/lag filter having a ratio of 6/12 will take longer to settle out than a filter having a ratio of 1/2.

Figure 3.25
Lead Dominated Filter (Ratio of 4/x)

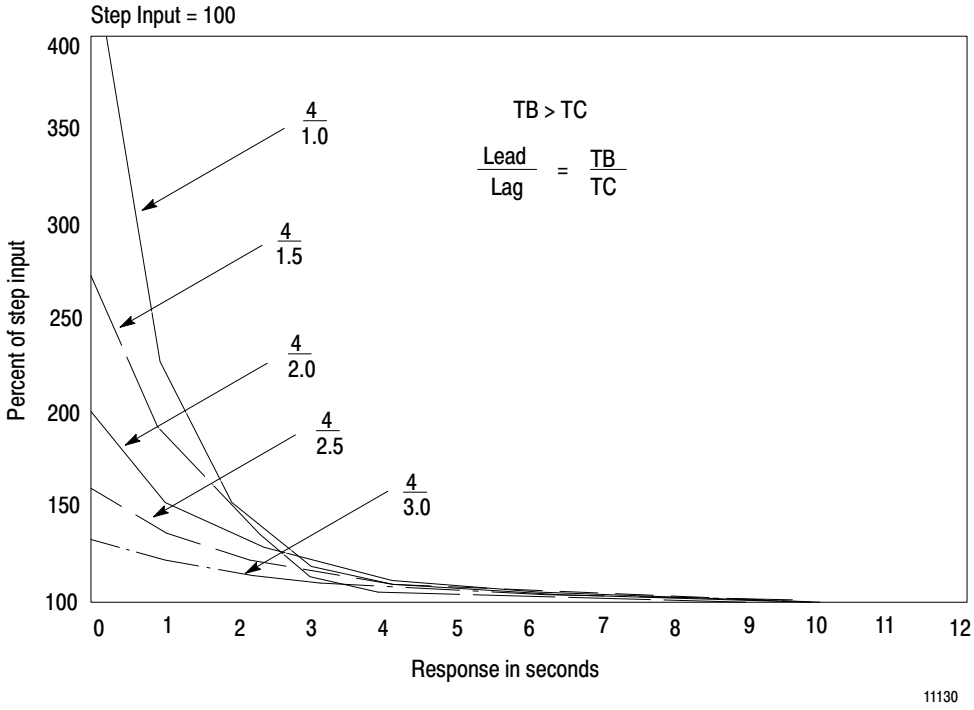
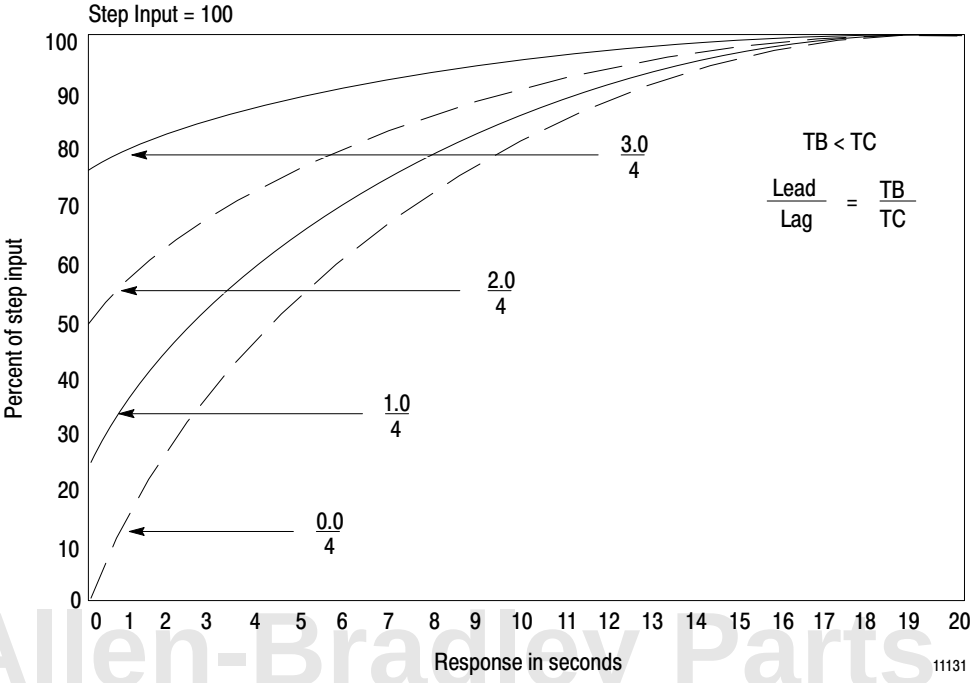


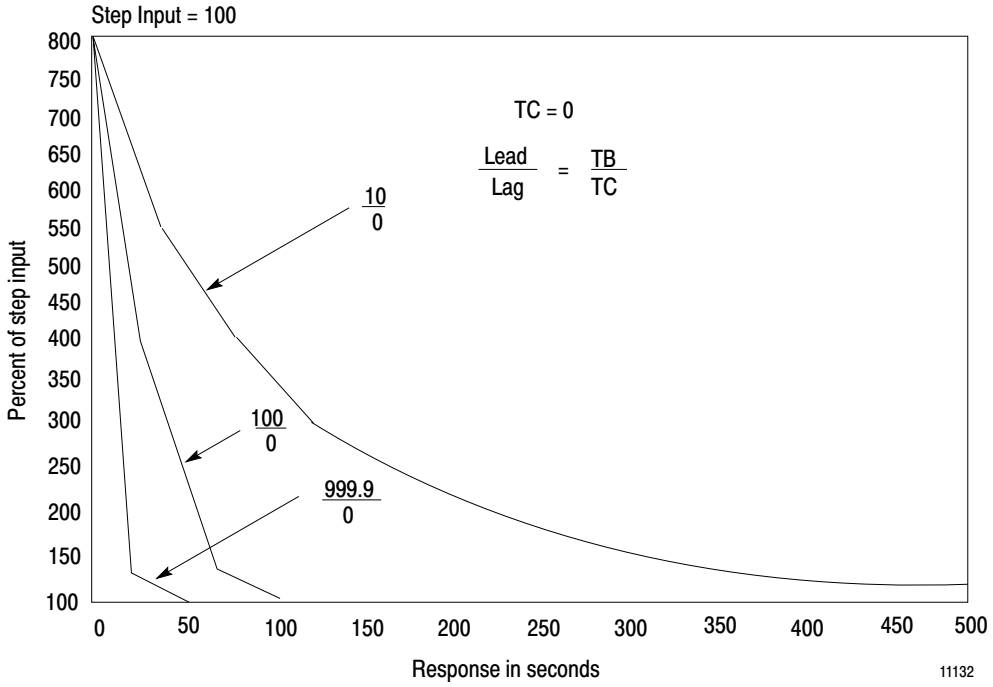
Figure 3.26
Lag Dominated Filter (Ratio of x/4)



Finally, the lead/lag ratio determines the initial response of the filter to a step input. For example, a lag dominated filter of 2/4 will respond with an initial step change of half the step input value. A lead dominated filter of 4/2 will respond with an initial step change of twice the step input value. The filter response to the step change cannot exceed eight times the step input value if the lead/lag ratio should exceed 8:1 (Figure 3.27).

To select the lead/lag feature, W30(W50)B05 must be set to 1. The lead value time constant TB and the lag value time constant TC must be set in the appropriate word. A value of zero entered for either the lead or lag value disables that function

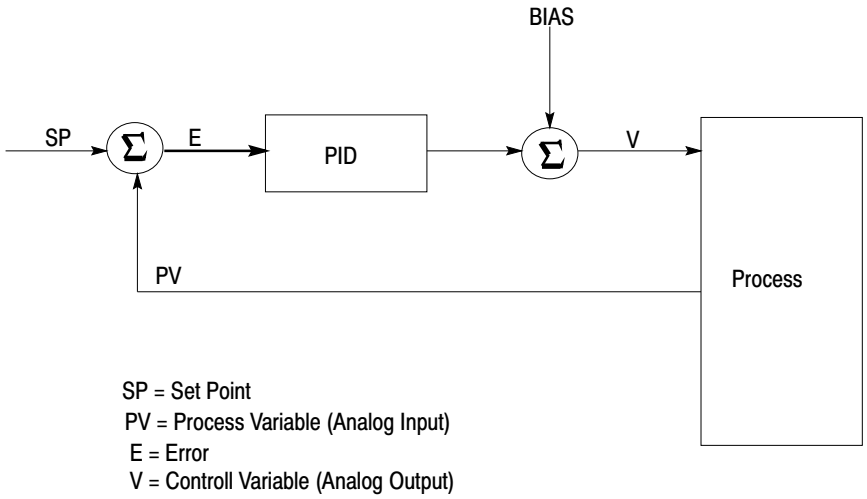
Figure 3.27
Lead Filter (Lag Function Disabled)



Closed Loop Control

Standard PID closed loop control is shown in Figure 3.28. the module compares the process variable input with the desired setpoint. The resultant error is operated upon by any selected combination of proportional, integral or derivative functions. The PID function adjusts the output to bring the process variable equal to the setpoint.

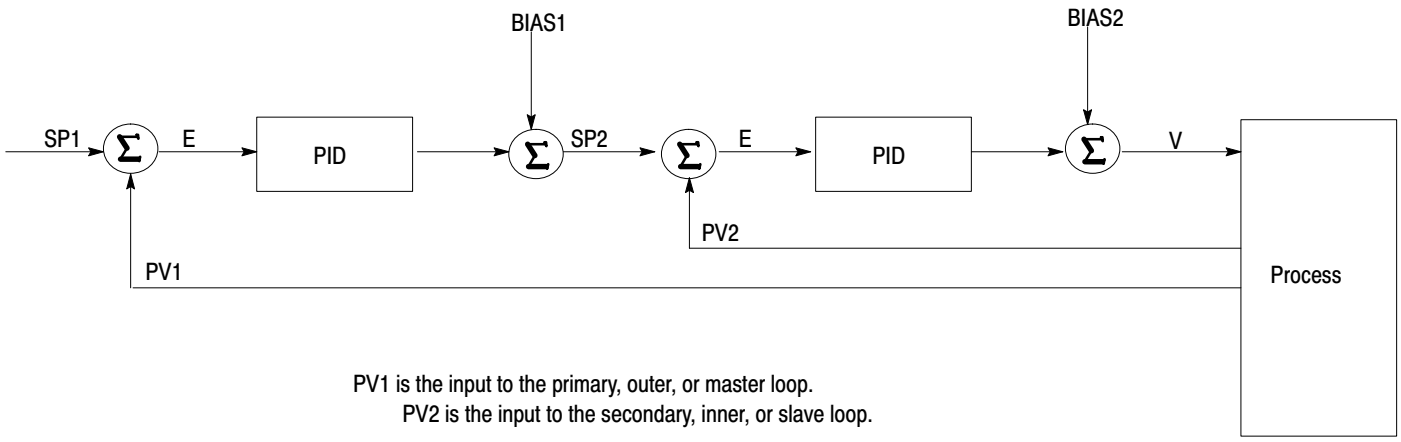
Figure 3.28
Closed Loop Control



Cascade Control

Cascade control is shown in Figure 3.29. There are two separate PID loops. The output of loop 1 is cascaded into the setpoint of loop 2. To enable direct cascade, set B00 = 1 in word W30(W50). Loop 1 is called the outer loop, master loop or primary loop. Loop 2 is called the inner loop, slave loop or the secondary loop. The inner loop senses a change and compensated for it before the outer loop is affected. This type of control is used to reduce the response time of the secondary loop when controlling a primary loop with large inertia.

Figure 3.29
Cascade Control



PV1 is the input to the primary, outer, or master loop.
PV2 is the input to the secondary, inner, or slave loop.

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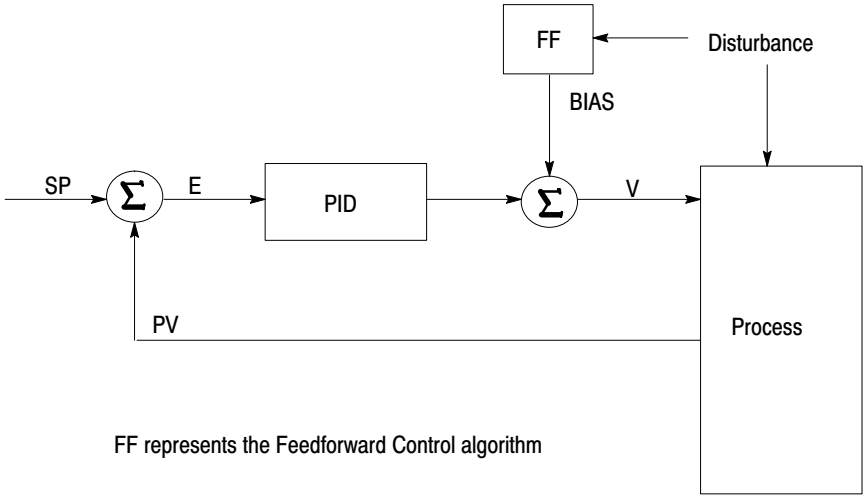
Feedforward Control

Feedforward control is shown in Figure 3.30. A disturbance is fed forward to the PID module to change the output before the disturbance changes the process variable. The PID module can perform one or more of the following functions on the feedforward input: square root, lead/lag, multiplication by a gain constant, and add an offset. Feedforward is often used to control processes with transportation lag.

Figure 3.30
Feedforward Control



FF represents the Feedforward Control algorithm

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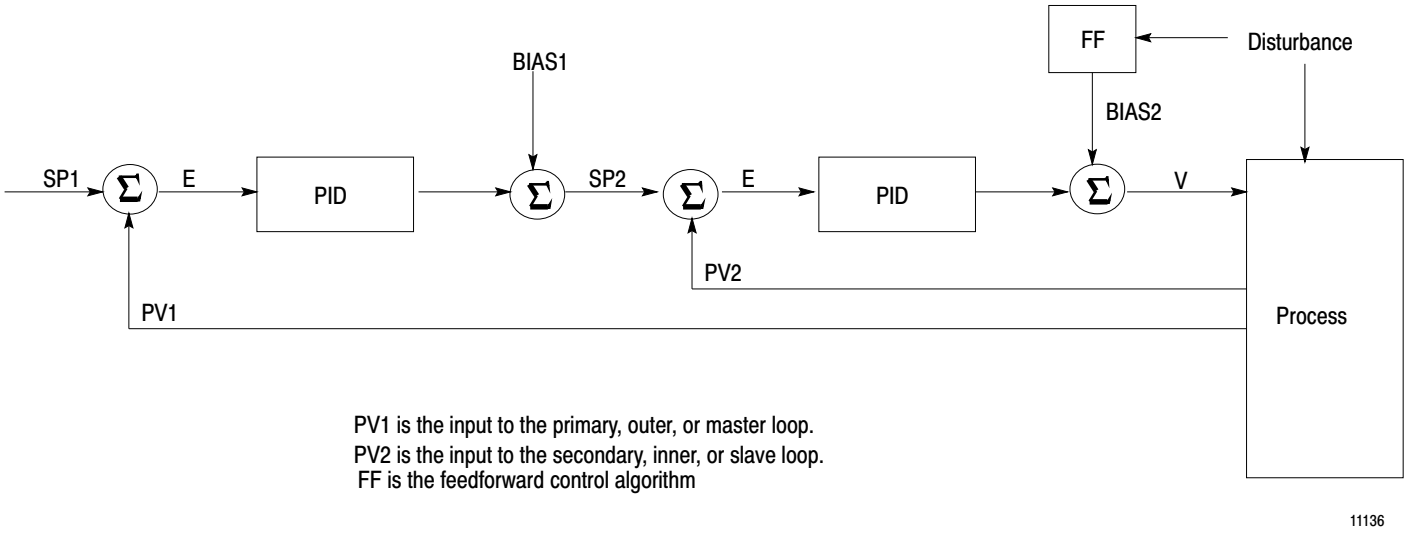
Cascade With Feedforward Control

Cascade with feedforward control is shown in Figure 3.31. The output of loop 1 is cascaded into the setpoint of loop 2. Loop 2 feedforward features are being used.

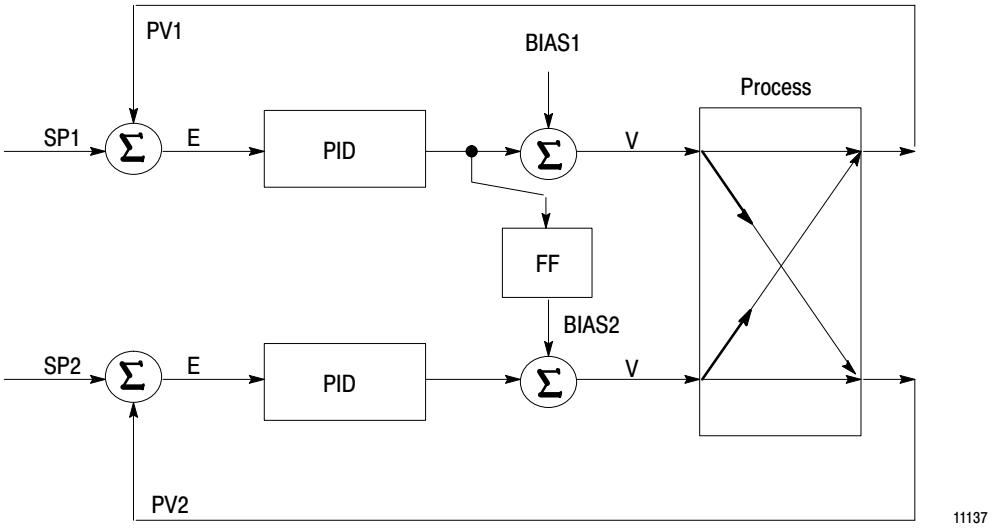
Figure 3.31
Cascade with Feedforward Control



Decouple Control (Multi-Loop, Multi-Variable)

Decoupling is shown in Figure 3.32. Decoupling is also known as multi-loop, multi-variable control. This type of control is required in some applications were there is interaction between loops. A change in loop 1 directly affects loop 2. Loop interaction is compensated by forwarding output data from loop 1 into the feedforward/input of loop 2. A change in the output of loop 1 adjusts the output of loop 2 without affecting the loop 2 PID calculation. Decoupling and cascade control can be used simultaneously. To enable decoupling, set W30(W50) B14 to 1.

Figure 3.32
Decouple Control



PC Processor Interactive Control

The PID module is a self-contained 2-loop process controller. Because the PC processor can program and monitor the PID module, there are numerous types of interactive control which can be performed. The following describes a few interactive control schemes.

If a process variable signal is required other than +4 to +20mA or +1 to +5VDC, another input module could be used to read the process variable. The PC processor could transfer this value to the PID module. For example, the PC processor could read a thermocouple input through the Thermocouple Input Module (cat.no. 1771-IX) and write the input value to the PID module.

The PC processor could also read digital inputs from transmitters with BCD output and transfer the information to the PID module. Block transfer timing must be considered.

The same applies to outputs. The analog output of the PID module can be read by the PC processor and written to another type of output module.

The PC processor can read analog inputs and set analog outputs. It can perform its own sophisticated PID control of many interactive loops. PID modules can function as analog I/O modules and be programmed for back-up. In the event of a PC processor failure or a break in communication with the PID module, PID modules can control their respective loops. The soft fault mode selection bit, W19(W39) B15, B14, B13 should be set to 1,0,0 respectively.

Adaptive gain control can be performed by the PC processor and PID modules. The C processor can change PID gain constants based on PID error values and external disturbances. Continuous processes can be fine tuned. Batch processes can be sequenced.

The fine tuning of a PC processor interactive system can depend on the remote scan time and length of user program. Tuning should be done in the fully operating system. If another model PC processor is substituted, the system may have to be returned.

Programming Recommendations for Start-up

When initializing an unprogrammed PID module, we recommend that you program only the minimum required rungs (Figure B.2 and Figure B.6) and load only the minimum data necessary. Then add PID control parameters (Dynamic block and loop block data) using on-line data change or the module's soft fault mode.

Load only the following data, setting all other data words and bits to zero.

Word W01	Bit 17 = 1, Bit 16 = 1, Bit 07 = 1 Set Bit 15 to 1 if using one loop. Set Bit 15 to 0 if using two loops.
Word W03	Load the dynamic block start address.
Word W04	Load the Loop 1 block start address.
Word W11	Load the Loop 2 block start address, if using two loops.
Word W18	Bit 16 = 1

Word W38 Bit 17 = 1 if using two loops.

Download this data to the module using the load/enter sequence. The module initializes and waits for PID control parameters. If not, refer to error codes in W60.

Add PID control parameters by a single load/enter sequence using the module's soft fault mode. We recommend using this method when your PID module is connected to a live process because you can load data table files in advance, and download them in one operation.

- Reset to 0 the module's soft fault reset bit, W01 B10.
- Place the processor in program mode.
- Load PID control parameters into the data table.
- Set to 1 the module's soft fault reset bit, W01 B10.
- Put the processor in run or run/program mode.
- Initiate the load/enter sequence.

You may also add PID control parameters one word at a time in run mode using on-line data change. We recommend using this method when your PID module is not connected to a live process because the PID module operates with partial data until configuration is complete. Refer to the Programming and Operations Manual of your processor for the procedure to change data on-line.

Once you have downloaded PID control parameters to the PID module, use on-line data change to adjust or tune existing loops.

Chapter 4

Troubleshooting

General

This chapter contains two troubleshooting guides. One describes how to interpret the LED indicators on the front of the PID module (Table 4.A). The second troubleshooting guide provides assistance when a programming error is encountered (Table 4.B).

LED Troubleshooting Guide

The operational status of the module is continuously indicated by the front panel LED indicators. Their status can be off, on, flashing or toggling. Flashing is defined as a condition affecting only one of the indicators when the other two are not changing. Toggling is defined as a condition where two indicators are alternately turning on and off.

Program Troubleshooting Guide

Probable causes of programming errors, indication of these errors, and recommended corrective action are listed in Table 4.B.

Be sure to read Programming Recommendations for Start-Up (chapter 3).

Table 4.A
LED Troubleshooting Guide

Indication	Description	Probable Cause	Recommended Action
○ FAULT ● RUN ○ STANDALONE	Normal Condition	Module is programmed and is executing normal control	
○ FAULT Ⓕ F RUN ○ STANDALONE	Module is un-programmed	On-board RAM has been cleared due to one of the following conditions: A) +5V DC power to digital circuitry has been interrupted, then restored to module. B)Module has been powered and is waiting for the initial load/enter sequence to be completed without error.	A)Initiate load/enter sequence to re-load RAM and to clear the condition. B)Check word W60 (diagnostic word) in order to determine which words are in error.
○ FAULT ○ RUN Ⓕ F STANDALONE	Module is in standalone mode in response to a soft fault.	A condition exists (or did exist) which caused the I/O to reset. A)Processor is in program or test mode. B)I/O fault has interrupted processor-to-module communication. C)PC processor faulted.	W01 Bit B10 must be energized in order to reset this condition. A)Switch processor to run mode. B)Check adapters, power supplies, communication cables and correct the condition. C)Refer to appropriate PC processor troubleshooting guide and correct the condition.
● FAULT Ⓧ X RUN Ⓧ X STANDALONE	Hardware fault in module	A)Module hardware faulted.	A)Cycle +5v DC digital power to module to clear the fault. If fault condition persists, replace PID module.
○ FAULT Ⓣ T RUN Ⓣ T STANDALONE	Indicates loss of ±15v DC power to analog circuitry	A)Wiring error. B)±15V DC supply is out of spec or failed.	A) Check all wiring from ±15V DC supply to field wiring arm. B)Adjust supply or replace it.
○ FAULT ○ RUN ● STANDALONE	Indicates a block transfer communication error	A)Block transfer rungs are incorrectly programmed. B)Illegal values are in words W03, W04 or W11.	A)Correct block transfer rungs B)Insert valid addresses.

LEGEND: ON, OFF, F FLASHING, T TOGGLING, X DON'T CARE

Table 4.B
Program Troubelshooting Guide

Indication	Probable Cause	Corrective Action
Incorrect analog input, tieback input, PV input	Programming plugs for conditioning the inputs are selected incorrectly. BCD or binary format is chosen incorrectly Transmitter is mis-calibrated.	Re-check programming plug selection. See section titled Internal Selections. Re-check W01 B12, B11 for BCD or binary format. Re-check range and span of transmitter.
Incorrect analog output	As above Actuator is miscalibrated.	As above Re-check actuator.
Loss of PV input bit is set	PV from analog input is not being received. PV from PC processor is not being received. (The loss of PV input is reported if no signal is present).	Check signal wiring, module and transmitter power supplies and input conditioning. Jumper PV (+LEAD) to +15V DC power connection. (Loss of pV is reported whether or not the PC processor is downloading the analog input).
Block transfer does not occur	Ladder diagram program contains an error.	Check that the block transfer instruction module address matches the PID module's location in the I/O rack. Check pre-conditioning of block transfer rungs. Verify that the program is similar to the example program in the appendix. Check bits B17 and B16 in the first word of each write block transfer to ensure proper settings for dynamic, loop 1, and loop 2 blocks. Check block start address words for correspondence to data table file locations.

Chapter 5

Calibration

General

The PID module is calibrated before it leaves the factory. The calibration of the module should be checked yearly. It can be returned to Allen-Bradley Systems Division for factory calibration. Revision B and later models can be calibrated using the procedures described in this chapter.

Test Equipment

The following test equipment and parts should be available. Some of this equipment can be borrowed from the system installation or an independent test station can be used.

DC Voltage Standard +10V, 0.1mV resolution	Fluke 342A, or equivalent
Digital Voltmeter 5 1/2 digit, 0.01% accuracy	Keithly 191, Fluke 8300A, or equivalent
Precision Resistor	Allen-Bradley Systems Division
250 ohms +0.02% 1/4 watt	PN 610996-01
Resistor 1000 ohms +l% watt	numerous sources
Industrial Terminal	Allen-Bradley system terminal or spare, compatible with test PC.
Programmable Controller	System PC or space
Analog Power Supply	Allen-Bradley Power Supply (cat. no. 1770-P1) +15V dc, -15V dc, system supply or spare
Chassis Power Supply	Allen-Bradley (cat. no. 1771-P2) system supply or spare
I/O Chassis	Allen-Bradley (cat. no. 1771-A1,-A2 or -A4) system chassis or system spare
Extender Board	Allen-Bradley (cat. no. 1771-EX)
Field Wiring Arm	Allen-Bradley (cat. no. 1771-WF) system spare
Alignment Tool “pottweeker”	Newark Electronic PN 35F616 or TV duplex Aligner with plastic shaft, or equivalent

Potentiometer Sealant	Organic Products “Torque Seal” P.O. Box 428, Irving, Texas 75060, or equivalent
Jumper Clips	E-Z Mini Hook Jumper 204-6w E-Z Mini Hook P. O. Box 450 Arcadia, CA 91006 or equivalent

Preparation

Disassemble the module by removing the left and right cover plates. The left-hand board is the digital board. The right hand board under the cover plate with the terminal identification label is the analog board. Be careful not to bend the three stake pins when separating the boards.

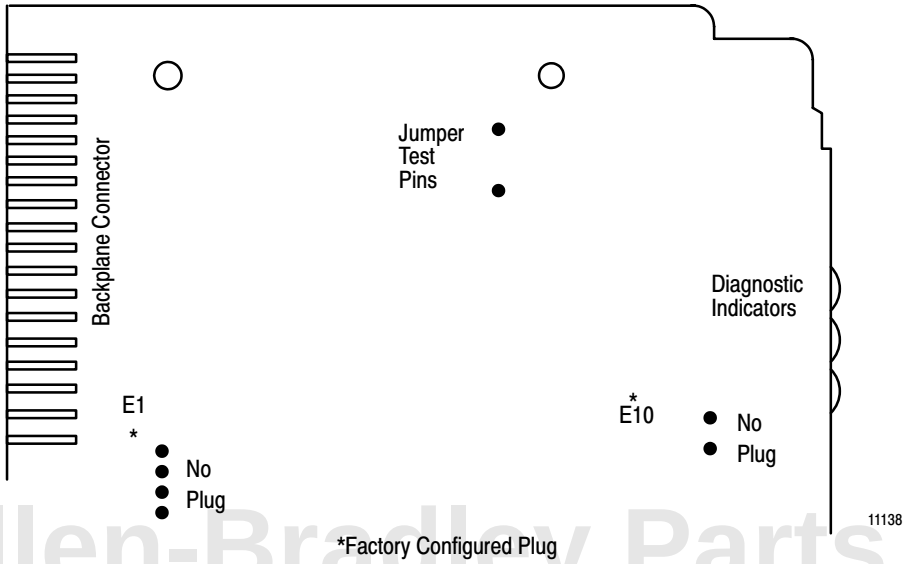
Extender Board and Jumper Clips

The analog and digital boards must be inserted in an I/O chassis during calibration so that data can be transferred between PC processor and module.

The analog board must be connected to the extender board to allow access to the test points and programming plugs.

Jumper clips or the equivalent must be used to jumper the pair of test pins on the digital board. The test pins are located at the top of the digital board near the center between IC numbers 4 and 5, Figure 5.1.

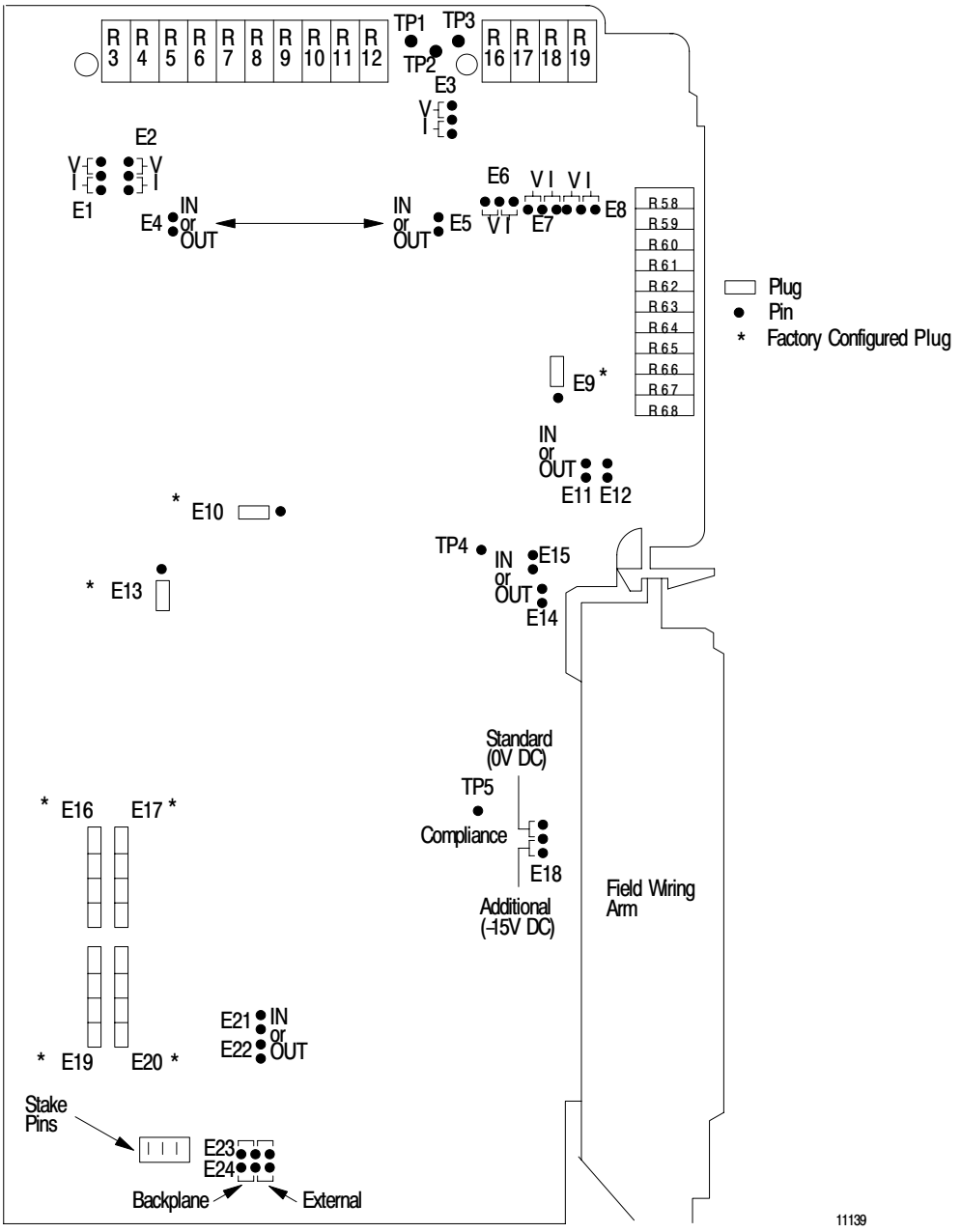
Figure 5.1
Jumper Pin Location (Digital Board)



Installation

Before installing the analog circuit board in the I/O chassis for calibration, record the initial positions of the programming plugs on . The programming plugs should be returned to these positions at the completion of the calibration procedure.

Figure 5.2
Calibration Locations (Analog Board)



NOTE: The programming plug positions referred to in the calibration procedures are upper/lower or left/right as viewed on the installed analog board. This refers to the plug position when inserted on two pins of a 3-pin group. The IN or OUT position referred to in the procedure refers to a 2-pin group where the plug is either fully inserted or inserted on only one of two pins, electrically floating. Refer to Figure 5.2 for the locations of the programming plugs, potentiometers and test points.

1. Turn off power to the I/O chassis.

2. Connect the analog circuit board to the extender board and install them in the right-hand slot (slot 1) of a module group.

3. Set the programming plug positions on the analog board for voltage mode.

E3 (E1) V, upper position
E5 (E4) IN position
E6 V, left position
(E2) upper position
E8 (E7) V, left position
E18 upper position, standard compliance

4. Locate and jumper the pair of test pins on the digital circuit board. Install the digital circuit board in the adjacent left-hand slot of the same module group.

5. Connect +15V dc and +5V dc power supplies. Be sure the programming plugs E23 and E24 are set for your source of +5V dc, backplane or external supply. Be sure all other I/O are disconnected from the PID module.

WARNING: All inputs and outputs (except for the +15V dc, -15V dc, +15V dc COMMON, +5V dc and +5V dc COMMON terminals) must be disconnected from the PID module during calibration. If connected to the system, unexpected machine operation could occur with possible damage to equipment and/or injury to personnel.

---

6. Install a PC processor whose memory, containing a 256 word data table, has been cleared.

7. Turn on +5V dc and +15V dc power supplies. Allow 15 minutes warm-up time for module stabilization.

8. Using an industrial terminal, enter the calibration program (Figure 5.2) into the PC processor. The PC processor must be in program mode.

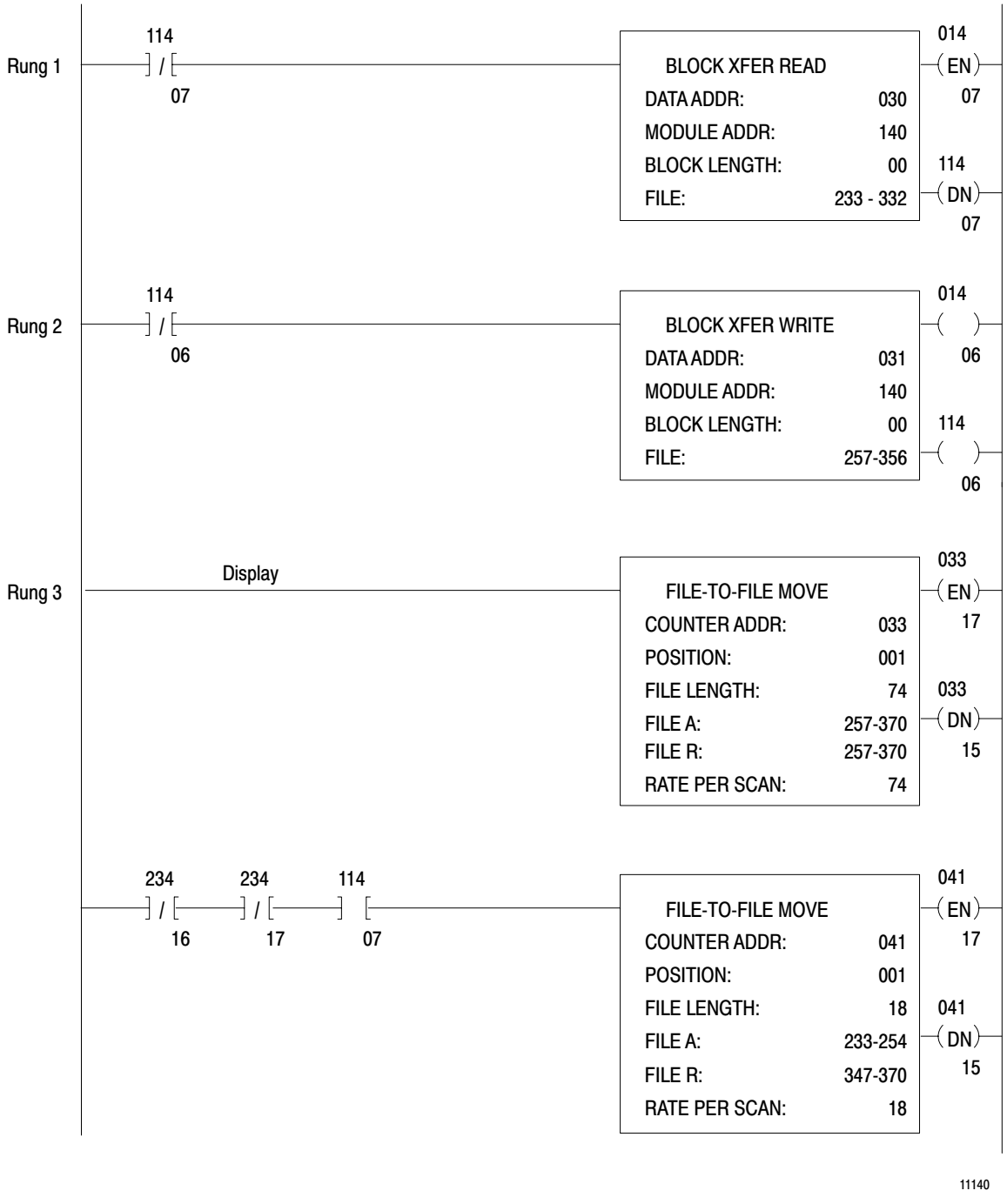
Calibration Program

The calibration program in Figure 5.3 can be adapted for use with any Allen-Bradley programmable controller capable of executing a block transfer program using block format instructions. This program is written for a Mini-PLC-2/15 or PLC-2/30 processor.

The calibration program continuously toggles between read and write block transfers. Be sure that the module address entered in the block instruction corresponds to the module's location in the I/O chassis. The calibration program's module address is rack 1, module group 4, slot 0. The block lengths have been set to the default value, 00. The file-to-file move instruction is used to display dynamic block, loop block and status block data.

NOTE: The user program must not be operating during calibration because it will interfere.

Figure 5.3
Calibration Program



Either a spare PC processor can be used (memory is blank) or system PC processor can be used after the user program has been erased from memory. The user program should first be recorded on cassette tape or digital cartridge so it can be reloaded after calibration.

Display of Hex Value

During the calibration procedure, hex values transferred to and from the PID module can be displayed by using the industrial terminal in data monitor mode. With the processor in program mode and the cursor on the file-to-file move instruction, press (DISPLAY) (1). The block files will be displayed in hex notation starting with word W01 in position 001.

The status words which must be monitored during calibration have the same number as the file positions. Disregarding the prefix W, the following status words can be monitored at the positions stated in Table 5.A.

These words can be displayed by pressing the key sequence (DISPLAY)(0)(6)(4). Word 064 will be displayed at the top of the industrial terminal screen.

Table 5.A
Monitor Words

Word	Title
W64	Analog input 1
W66	Tieback input 1
W71	Analog input 2
W73	Tieback input 2

Setting Word Values

When using the industrial terminal in the data monitor mode, the word intensified by the field cursor is duplicated in the command buffer at the bottom of the screen. Enter word values as follows using on-line data change. With the processor in run/program mode and the ladder diagram displayed, cursor to the file-to-file move instruction. Press the key sequence (SEARCH)(5)(1)(DISPLAY)(1). The block files will be displayed starting with position 001. Place the field cursor on the data of a word using the (SHIFT)(>), (SHIFT)(<),(^) and/or (v) keys as needed. Enter or change data through the command buffer using the alphanumeric, (>) and (<) keys as needed. After the desired value has been entered in the command buffer, press the (INSERT) key to load this value into the PC processor memory. The value will be block transferred to the PID module immediately. The on-line entry of data can be terminated at any time by pressing (CANCEL COMMAND) twice.

Control bits can be set by loading hex values into control words. Hex values which must be set as part of the calibration procedures are listed in Table 5.B and described in a. through d. as follows:

a. Calibration bit B13 in word W01 must be set at module power up to place the PID module in calibration mode. Load C800 hex into word W01.

b. The input to be calibrated in sections titled Voltage Reference and Current Inputs through section titled Output Amplifier, Voltage Adjustments is selected by loading the corresponding hex value into word W02.

c. The full-scale SET OUT value of OFFF hex must be loaded into word W05 for loop 1 (1 word W12 for loop 2) for calibration procedures in sections titled Current Inputs and Tieback Current Inputs.

d. The set output bit B01 for loop 1 (B02 for loop 2) must be set in word W01 to download the SET OUT value of OFFF hex to the PID module in calibration procedures in sections titled Current Inputs and Tieback Current Inputs.

Table 5.B
Calibration Values

Description	Procedure	Word	Hex Value	
Calibration bit	Power up	W01	C800	
Input select	5.4.2		**A-B**	**ISA**
analog input 1	and	W02	0000	0001
tieback input 1	5.4.5	W02	4000	4001
analog input 2	thru	W02	8000	8001
tieback input 2	5.4.7	W02	C000	C001
SET OUT value	5.4.5			
loop 1	and	W05	OFFF	
loop 2	5.4.6	W12	OFFF	
Set Output bit	5.4.5			
loop 1	and	W01	C802	
loop2	5.4.6	W01	C804	

NOTE: When the dynamic block containing the calibration bit is first transferred after power up, the module automatically enters calibration mode. Place the module in calibration mode as follows:

- set W01 B13 by loading C800 hex into word W01
- cycle backplane power to the PID module

Calibration Procedures

Module calibration consists of the following seven procedures.

1. Voltage reference
2. A/D offset error and gain error compensation
3. isolation amplifiers
4. output amplifiers, current mode
5. current inputs, +4 to +20mA
6. tieback inputs, +4 to +20mA
7. output amplifiers, voltage mode

Procedures 3 through 7 require the calibration of loop 1 followed by the calibration of loop 2 before starting the next procedure.

Calibration adjustments should be set to the exact values stated in the text except where a tolerance is given. Calibration readings should be made to $\pm$0.0002V dc.

Field wiring arm terminals are referred to in the calibration procedures as TERMINAL followed by a number.

Voltage Reference

Adjust the module's precision voltage reference to -10.0000V dc using the following procedure. The programming plugs should be set for voltage mode as described in section titled Installation

1. Connect the digital voltmeter as follows:

+ lead to TP2, Test Point 2
-lead to TERMINAL 8

2. Adjust R67 for a reading of -10.0000V dc.

A/D Offset Error and Gain Error Compensation

Using the following procedure, adjust the A/D comparator offset error to zero. Measure, record and compensate for the gain error.

1. Remove programming plug E18. Insert it on one pin, only (electrically floating). This will be referred to as the OUT position.

2. Move the programming plug E13 from the factory configured lower position to the upper position.

3. Enable the module's tieback input 1 by loading 4000 hex into word W02.

4. Monitor the tieback input word at position 066 for the next three adjustments.

5. Adjust R68 until the tieback input reading is 0001 hex.

6. Slowly adjust R68 by quarter turns until the tieback input reading just decreased to 0000 hex.

7. Place programming plug E-13 in the OUT position.

8. Connect the DC voltage standard as follows, set to 10.0000V dc.

+lead to middle pin of E13
-lead to TERMINAL 8

9. Carefully adjust the DC voltage standard until the tieback input reading at 066 just begins to read OFFF hex. Record this value as full-scale V_{AD}.

10. Subtract 10.0000V dc from the full-scale V AD value in step 9. Record this value as ^V. It will be positive or negative.

$\triangle V = V_{AD}$ -10.000V dc

11. Calculate the common mode calibration voltage and record the value. It will be used in step 15.

$$CMV = 2.50V\ dc + \triangle \frac{V}{4}$$

12. Jumper TERMINAL 11 to 14.

13. Reconnect the D

C voltage standard as follows, set to the CMV voltage from step 11.

+lead to TERMINAL 8
-lead to TERMINAL 11

14. Connect the digital voltmeter as follows (the reading will be negative):

+lead TP3
-lead TERMINAL 8

15. Adjust R58 until the CMV (negative) voltage from step 11 is obtained at TP3.

16. Remove the DC voltage standard.

17. Place the E18 programming plug in the standard compliance upper position.

18. Remove the jumper from TERMINALS 11 AND 14.

19. Reconnect the DC voltage standard as follows, set to +1.0000V dc

+lead to TERMINAL 14
-lead to TERMINAL 8

20. Reconnect the digital voltmeter as follows:

+lead to TP3
-lead to TERMINAL 8

21. Adjust R18 for a reading of 0.0000V dc.

22. Reconnect the DC voltage standard as follows, set to +5.0000V dc.

+lead to TERMINAL 14
-lead to TERMINAL 8

23. Adjust R17 until the full scale VAD voltage recorded in step 9 is obtained.

24. Return the E13 programming plug to its factory configured lower position.

Isolation Amplifiers

Using the following procedure, adjust the offset to zero, gain to 1, and optimize common mode rejection. Loop 2 information is presented in parentheses, ie (loop 2). The loop 2 procedure should not be started until the entire procedure for loop 1 has been completed.

1. Jumper TERMINALS 17 and 18 (15 and 16) to TERMINAL 8.

2. Connect the digital voltmeter as follows:

+lead to TP4 (TP5)
-lead to TERMINAL 8

3. Adjust R19 (R16) for a reading of 0.0000V dc.

4. Remove the jumper from TERMINAL 17 (15), only.

5. Connect the DC voltage standard as follows, set to +5.0000V dc.

+lead to TERMINAL 8
-lead to TERMINAL 17 (15)

6. Adjust R62 (R59) for a reading of +5.0000V dc.

7. Remove jumpers. Jumper TERMINAL 17 to 18 (15 to 16).

8. Reconnect the DC voltage standard as follows, set to +5.0000V dc.

+lead to TERMINAL 8
-lead to TERMINAL 18 (16)

9. Connect the digital voltmeter as follows:

+lead to TP4 (TP5)
-lead to TERMINAL 8

10. Adjust R63 (R60) for a reading of zero at TP4 (TP5).

11. Repeat the procedure for loop 2.

Output Amplifiers, Current Mode

Using the following procedure, configure the output circuits to current mode and adjust the scaling resistors for correct lower and upper output limits. At the same time, adjust for a minimum effect on the output due to changes in load resistance. The adjustments are interactive and must be repeated until the interaction is minimized. Complete the procedure for loop 1 before beginning the procedure for loop 2.

1. Set 1 - Set the programming plug positions for current mode. Refer to Figure 5.1.

E3 (E1) I, lower position
E6 I, right position
(E2) lower position
E8 (E7) I, right position
E18 lower position for additional compliance.

2. Turn off +5V dc.

3. Place E (E4) in the OUT position.

4. Connect the 1 K and 250 ohm precision resistors in series between TERMINAL 12 (10) And TERMINAL 11.

5. Connect the digital voltmeter across the 250 ohm resistor as close to the resistor body as possible.

   +lead to the TERMINAL 12(10) side of the resistor
   -lead to the TERMINAL 11 side of the resistor

6. Adjust R10 (R6) for a reading of +5.000V dc across the resistor.

7. Short the lK resistor.

8. Adjust R9 (R4) for a reading of +5.000V dc across the resistor.

9. Place E5 (E4) in the IN position, inserted on both pins.

10. Adjust R8 (R3) for a reading of 1.000V dc across the resistor.

11. Place E5 (E4) in the OUT position.

12. Read the voltage across the 250 ohm resistor. It should be 5.000V dc +2.5mV.

13. Remove the short across the 1K resistor.

14. Repeat steps 6 through 12 until steps 10 and 12 are satisfied without further adjustment.

15. Repeat the procedure for loop 2.

16. Turn on +5V dc. Return E4 and E5 to their initial positions, IN or OUT as recorded in section titled Installation.

Current Inputs

Using the following procedure with the input circuits configured to current mode, adjust the input scaling resistor to produce a full-scale reading from the A/D converter for a 20mA input. Repeat the procedure for the loop 2 input after loop 2 has been completed.

1. Place E14 (E15) in the IN position.

2. Jumper TERMINAL 12 TO 18 (12 TO 16).

3. Jumper TERMINAL 17 (15) to 11.

4. Enable the module's analog input by loading 0000 hex into word W02 for loop 1 (8000 hex for loop 2).

5. Load a value of OFFF hex into W05(W12) for a full-scale analog output. Set the set output bit by loading C802 hex into W01 for loop 1 (C804 for loop 2).

6. Monitor analog input 1 in position 064 for loop 1 (analog input 2 in position 071 for loop 2).

7. Adjust R64 (R61) until the reading of the analog input just becomes OFFF, hex.

8. Repeat for loop 2.

9. Place E14 (E15) in its initial position, IN or OUT, and remove the jumpers from the field wiring arm.

Tieback Current Inputs

Using the following procedure with the input circuits configured to current mode, adjust the input scaling resistor to produce a full scale reading from the A/D converter for a 20mA input. Repeat the procedure for the loop 2 input after loop 1 had been completed.

1. Place E11 (E12) in the IN position.

2. Jumper TERMINALS 12 and 14 (12 and 13).

3. Enable the module's tieback input by loading 4000 hex into word W02 for loop 1 (C000 hex for loop 2).

4. Load a value of OFFF hex into W05 (W12) for a full-scale analog output. Set the set output bit by loading C802 hex into word W01 for loop 1 (C804 for loop 2). Refer to Figure 5.2 if necessary.

5. Monitor tieback input 1 in position 066 for loop 1 (tieback input 2 in position 073 for loop 2).

6. Adjust R66 (R65) until the tieback input reading just becomes OFFF hex.

7. Repeat for loop 2.

8. Place E11 (E12) in its initial position, IN or OUT, and remove the jumper from the wiring arm.

Output Amplifier, Voltage Adjustments

Using the following procedure, configured the amplifier circuits to voltage mode and adjust the outputs to 1.000V dc and 5.000V dc for programmed values of 0 and full scale, respectively.

1. Set the programming plug position for voltage mode.

E3 (E1) V, upper position
E5 (E4) IN position
E6 V, left position
(E2) upper position
E8 (E7) V, left position
E18 upper position, standard compliance

2. Connect the digital voltmeter as follows:

+lead to TERMINAL 12 (10)
-lead to TERMINAL 8

3. Adjust R11 (R5) for an output voltage reading of 1.000V dc.

4. Change E5 (E4) to the OUT position. Turn off +5V dc.

5. Adjust R12 (R7) for an output voltage of 5.000V dc.

6. Repeat for loop 2.

7. Set the programming plugs on the analog board to their initial positions as recorded in section titled Installation.

Module Re-assembly

Re-assemble the module using the following procedure.

1. Turn off +5V dc and +15V dc.

2. Remove the analog and digital circuit boards from the I/O chassis and disconnect the extender board from the analog board.

3. Apply pot sealer to the adjusting screws to indicate whether or not any of the pots had been adjusted between calibrations.

4. Remove the jumper from the digital board.

5. Check all programming plug locations on the analog board to ensure they are returned to their initial positions as recorded earlier in section titled Installation.

6. Carefully re-assemble the module. Be sure that the programming plug locations at E11 and E12, if in the OUT position, do not interfere with the front cover flange. Also be sure that the three stake pins mate with their respective sockets on the digital circuit board.

Appendix A

Worksheets

The following 5 worksheets should be reproduced as needed:

Worksheet 1: Dynamic Block

Worksheet 2: Loop 1 Block

Worksheet 3: Loop 2 Block

Worksheet 4: Status Block

Publication 5045: Data Table Map

Allen-Bradley Programmable Controller
1771-PD Module Worksheet 1
Dynamic Block

Page____ of ____

Project Name: _____ Processor: _____

Designer: _____ Data Table Size: _____

DATA TABLE WORD USAGE From____ to____

Data Table Word Address	Module Word #	Name	Value	Range	BCD or BIN	Multiplier	Sign
	[3]		17 14 13 10 07 04 03 00				
	W01	Master Control Word	1 1 0 0 0	FFFF	→		[4]
	W02	Control Word		F000	–		
	W03	Dynamic Block Start Address		FFFF	_		
	W04	Loop 1 Block Start Address		FFFF	_		
	W05	Set Analog Output 1 SET OUT1		4095	[1]		
	W06	Set Point 1 SP1		4095/ 9999	[2]	W19 B06 x10 x1	W19 B07 – + [5]
	W07	Proportional Gain 1 K_P1		99.99	_	W19 B05,04	[6]
	W08	Bias 1 BIAS1		9999	_		
	W09	Set Process Variable 1 SET PV1		4095	[1]		
	W10	Set Feedforward Input 1 SET FFI1		4095	[1]		
	W11	Loop 2 Block Start Address		FFFF	_		
	W12	Set Analog Output 2 SET OUT2		4095	[1]		
	W13	Set Point 2 SP2		4095/ 9999	[2]	W39 B06 x10 x1	W39 B07 – + [5]
	W14	Proportional Gain 2 K_P2		99.99	_	W39 B05, 04	[6]
	W15	Bias 2 Bias		9999	_		
	W16	Set Process Variable 2 SET PV2		4095	[1]		
	W17	Set Feedforward Input 2 SET FFI2		4095	[1]		

NOTES:
[1] denotes selection by W01 B12
[2] denotes selection by W01 B11
[3] also represents the displayed position number
[4] record Hex value
[5] circle choice
[6] record value

Allen-Bradley Programmable Controller
1771-PD Module Worksheet 2 Loop 1 Block

Page____ of ____

Project Name: _____ Processor: _____
Designer: _____ Data Table Size: _____

DATA TABLE WORD USAGE From____ to____

Data Table Word Address	Module Word #	Name	Value	Range	BCD or BIN	Multiplier	Sign
	[1]		17 14 13 10 07 04 03 00				
	W18	Loop 1 Control Word A	0 1	FFFF	→		[2]
	W19	Loop 1 Control Word B		FFFF	→		[2]
	W20	Input Filter Time Constant 1 TA1		99.99	--	x10 W19 B12 x1	[3]
	W21	Maximum Negative Error 1 EMN1		4095	--		
	W22	Maximum Positive Error 1 EMP1		4095	--		
	W23	Dead Band 1 DB1		4095	--		
	W24	Integral Gain 1 K_I1		9.999	--	W19 B03,02	[4]
	W25	Derivative Gain 1 K_D1		99.99	--	W19 B01,00	[4]
	W26	Integral Term Limit 1 V_IMAX1		9999	--		
	W27	Derivative Term Limit 1 V_DMAX1		9999	--		
	W28	Minimum Output Limit 1 VMIN1		4095	--		
	W29	Maximum Output Limit 1 VMAX1		4095	--		
			17 14 13 10 07 04 03 00				
	W30	Loop 1 Expanded Control Word		FFFF	→		[2]
	W31	Minimum Scaling Value 1 SMIN1		9999	--		W30 B04 – + [3]
	W32	Maximum Scaling Value 1 SMAX1		9999	--		W30 B03 – + [3] [6]
	W33	Feedforward Offset 1 FFO1		9999	--		
	W34	Feedforward Gain 1 K_F1		99.99	--	W30 B07,06	[4]

	W35	Lead Time Constant 1 TB1	| | |	99.99	--	x10 W19 B11 x1	3
	W36	Lag Time Constant 1 TC1	| | |	99.99	--	x10 W19 B11 x1	3

NOTES:
[1] also represents the displayed position number
[2] record Hex value
[3] circle choice
[4] record value

Allen-Bradley Programmable Controller
1771-PD Module Worksheet 3 Loop 2 Block

Page____ of ____

Project Name: _____ Processor: _____
Designer: _____ Data Table Size: _____

DATA TABLE WORD USAGE From____ to____

Data Table Word Address	Module Word #	Name	Value	Range	BCD or BIN	Multiplier	Sign
	[1]		17 14 13 10 07 04 03 00				
	W38	Loop 2 Control Word A	10	FFFF	→	9200 [2]	
	W39	Loop 2 Control Word B		FFFF	→	3820 [2]	
	W40	Input Filter Time Constant 2 TA2	| | |	99.99	--	x10 W39 B12 x1	3
	W41	Maximum Negative Error 2 EMN2	| | |	4095	--		
	W42	Maximum Positive Error 2 EMP2	| | |	4095	--		
	W43	Dead Band 2 DB2	| | |	4095	--		
	W44	Integral Gain 2 K_I2	| | |	9.999	--	W39 B03,02	4
	W45	Derivative Gain 2 K_D2	| | |	99.99	--	W39 B01,00	4
	W46	Integral Term Limit 2 V_IMAX2	| | |	9999	--		
	W47	Derivative Term Limit 2 V_DMAX2	| | |	9999	--		
	W48	Minimum Output Limit 2 VMIN2	| | |	4095	--		
	W49	Maximum Output Limit 2 VMAX2	| | |	4095	--		
			17 14 13 10 07 04 03 00				
	W50	Loop 2 Expanded Control Word		FFFF	→	E000 [2]	

	W51	Minimum Scaling Value 2 SMIN2	| | |	9999	--		W50 B04 – +	3
	W52	Maximum Scaling Value 2 SMAX2	| | |	9999	--		W50 B03 – +	3
	W53	Feedforward Offset 2 FFO2	| | |	9999	--			
	W54	Feedforward Gain 2 K_F2	| | |	99.99	--	W50 B07.06		4
	W55	Lead Time Constant 2 TB2	| | |	99.99	--	W39 B11 x10 x1		3
	W56	Lag Time Constant 2 TC2	| | |	99.99	--	W39 B10 x10 x1		3

NOTES:
[1] also represents the displayed position number
[2] record Hex value
[3] circle choice
[4] record value

Allen-Bradley Programmable Controller
1771-PD Module Worksheet 4 Status Block

Page____ of ____

Project Name: _____ Processor: _____
Designer: _____ Data Table Size: _____

DATA TABLE WORD USAGE From____ to____

Data Table Word Address	Module Word #	Name	Value	Range	BCD or BIN	Multiplier	Sign
			17 14 13 10 07 04 03 00				
	W57	For Future Use	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0000	→		
	W58	Alarm (Both Loops)		FFFF	→		
	W59	Next Block Start Pointer	| | |	FFFF	--		
	W60	Loop Time/Diagnostic	| | |	9999/ FFFF	--		
	W61	Status Loop 1		FFFF	--		
	W62	Error Loop 1 ERROR 1	| | |	9999	--		W61 B17 [2]
	W63	Read Loop 1 Output READ V1	| | |	4095	[1]		
	W64	Read Analog Input 1 READ IN1	| | |	4095	[1]		
	W65	Read Process Variable 1 READ PV1	| | |	9999	--		W61 B16 [2]
	W66	Read Tieback Input 1 READ TIE1	| | |	4095	[1]		
	W67	Read Feedforward Value 1 ReadFFV1	| | |	9999	--		W61 B13 [2]

	W68	Status Loop 2		FFFF	--		
	W69	Error Loop 2 ERROR2	| | |	9999	--		W68 B17 [2]
	W70	Read Loop 2 Output READ V2	| | |	4095	[1]		
	W71	Read Analog Input 2 READ IN2	| | |	4095	-- [1]		
	W72	Read Process Variable 2 READ PV2	| | |	9999	--		W68 B16 [2]
	W73	Read Tieback Input 2 READ TIE2	| | |	4095	[1]		
	W74	Read Feedforward Value 2 Read FFV2	| | |	9999	--		W68 B13

NOTES:

[1] Denotes selection by W01 B12
[2] If scaling was used, examine W19 to determine if x 10 was used.

Allen-Bradley Programmable Controller
Data Table MAP (128-word)
(Publication 5045 – February, 1982)

PAGE_____ OF_____
ADDRESS_____ TO_____

PROJECT NAME_____ PROCESSOR_____

DESIGNER_____ DATA TABLE SIZE_____

STARTING WORD ADDRESS
00

BIT NUMBER
17 10 07 00

DESCRIPTION

00																
01																
02																
03																
04																
05																
06																
07																
10																
11																
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72																

STARTING WORD ADDRESS
00

BIT NUMBER
00 10 07 00

DESCRIPTION

00																
01																
02																
03																
04																
05																
06																
07																
10																
11																
12																
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Appendix B

Application Example 1, Continuous Block Transfer

General

The example described in this appendix is a single closed loop temperature control application. Standard and/or expanded control features can be selected as required by the application. The program uses block transfer to maintain continuous communication between the PID module and the PC processor.

Following the program description, typical values of selected standard control features are introduced using a worksheet for the dynamic block and loop 1 block. Worksheets simplify record keeping associated with writing the program. Worksheet forms in appendix A should be reproduced and used as needed.

Example Application

A fluid or material is passed through a heat exchanger where its temperature is maintained at set point. A temperature transmitter, which outputs a +1 to +5V DC signal to the PID module, monitors the temperature of the fluid or material as it leaves the heat exchanger. The temperature is controlled by regulating the amount of thermal energy permitted into the heat exchanger. An manual control station is connected to provide manual backup to the control system (Figure B.1).

Program for PLC-2 Family Processors

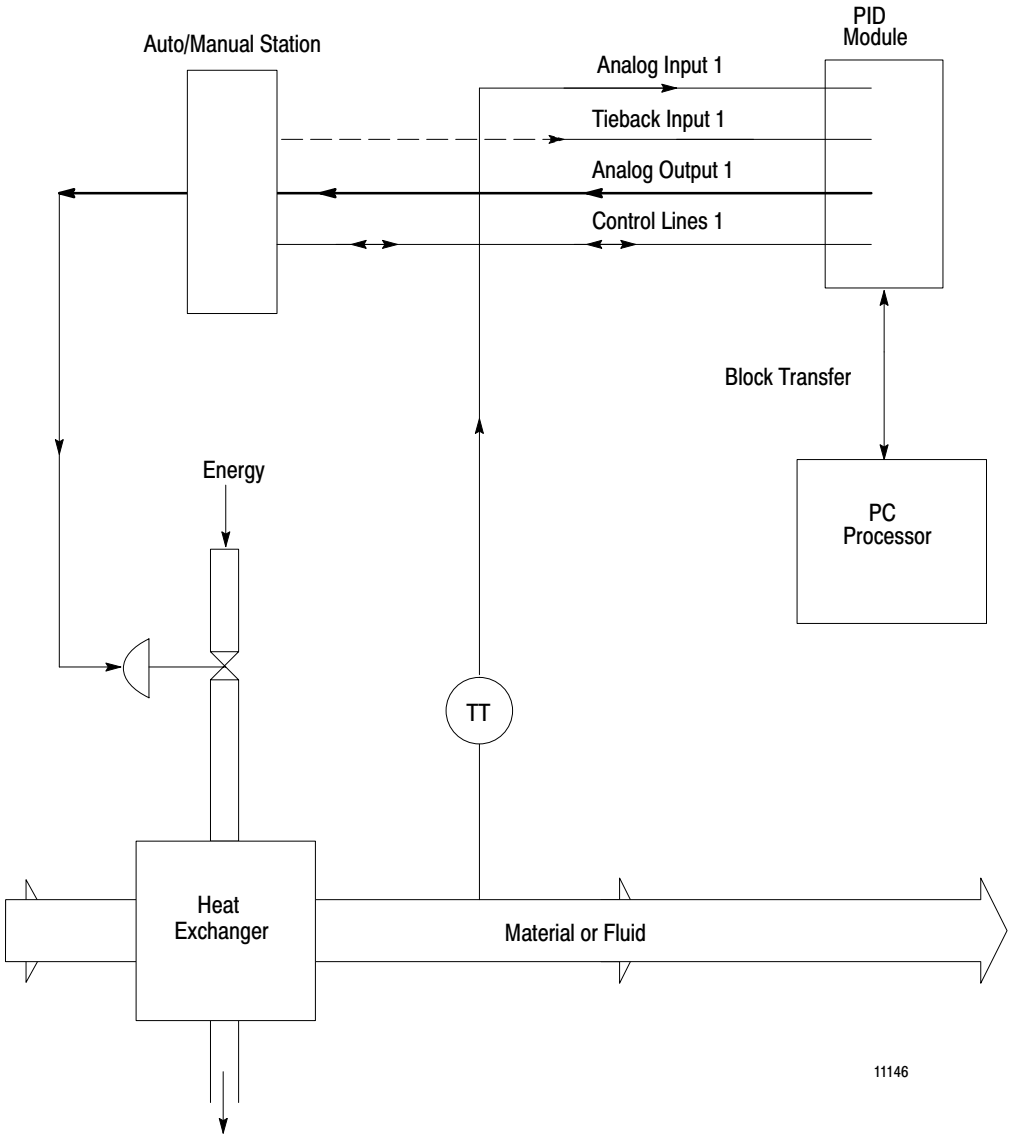
A ladder diagram program that can be used to control the single loop is presented in Figure B.2. The program is written for a Mini-PLC-2/15 or PLC-2/30 controller.

NOTE: The same program could be used if a second loop is required by the application. If used, loop 2 parameters would have to be entered into appropriate files. Bit W01 B15 would have to be set to zero in the master control word W01 to set the module for 2-loop operation.

This general ladder diagram program uses alternating read/write block transfers. During normal operation, dynamic block and status block data is continuously exchanged between the PID module and PC processor. This allows the latest process status to be read into the data table. This also allows data in the dynamic block to be written to the module

immediately upon entry into the data table. New dynamic block data may include manipulated status values, hardware inputs and data entered from the industrial terminal.

Figure B.1
Single Loop Temperature Control



If data in a loop block requires change at any time, a single load/enter sequence can be initialized by closing a pushbutton switch (111/00, rung 2). The load/enter sequence is initiated automatically at module power-up and during recovery from a power loss.

The program also allows manual control over the soft fault reset bit (W01 B10, 257/10) using a selector switch. When bit 257/10=1, the PID module automatically return to normal operation once the cause of a soft fault has been corrected. However, when bit 257/10=0 the PID module will not automatically return to normal operation when the cause of the soft fault is corrected. Return to normal operation must be manually initiated by closing switch 111/06. Manual soft fault reset allows the operator to determine the cause of the soft fault and review the current process status before returning control to the PID module.

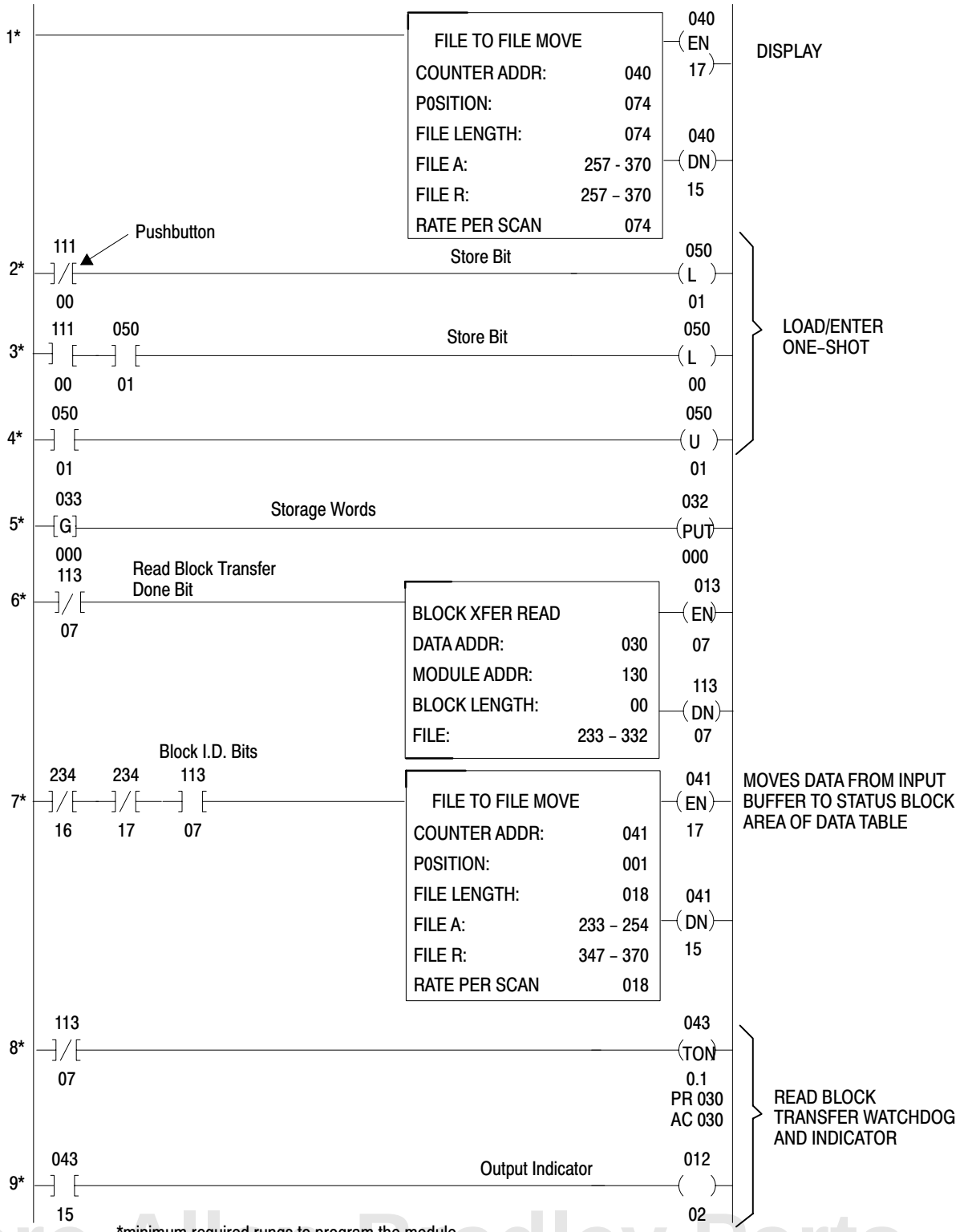
If, for some reason, the process variable signal becomes lost, the PID module would normally hold the analog output value existing at that moment. As an alternative, in this application the ladder diagram program automatically sets the output to a stored value upon loss of the process variable signal. The program examines the loss of input bit (W61 B07) and sets the output 1 bit (W01 B01). This sets the analog output to the value stored in W05.

Indicators have been programmed to illuminate if any of the following conditions should occur:

- the manual control station is in manual mode
- communication between PID module and PC processor is delayed or lost
- the PID module is powered and waiting for a load/enter sequence
- the load/enter sequence failed

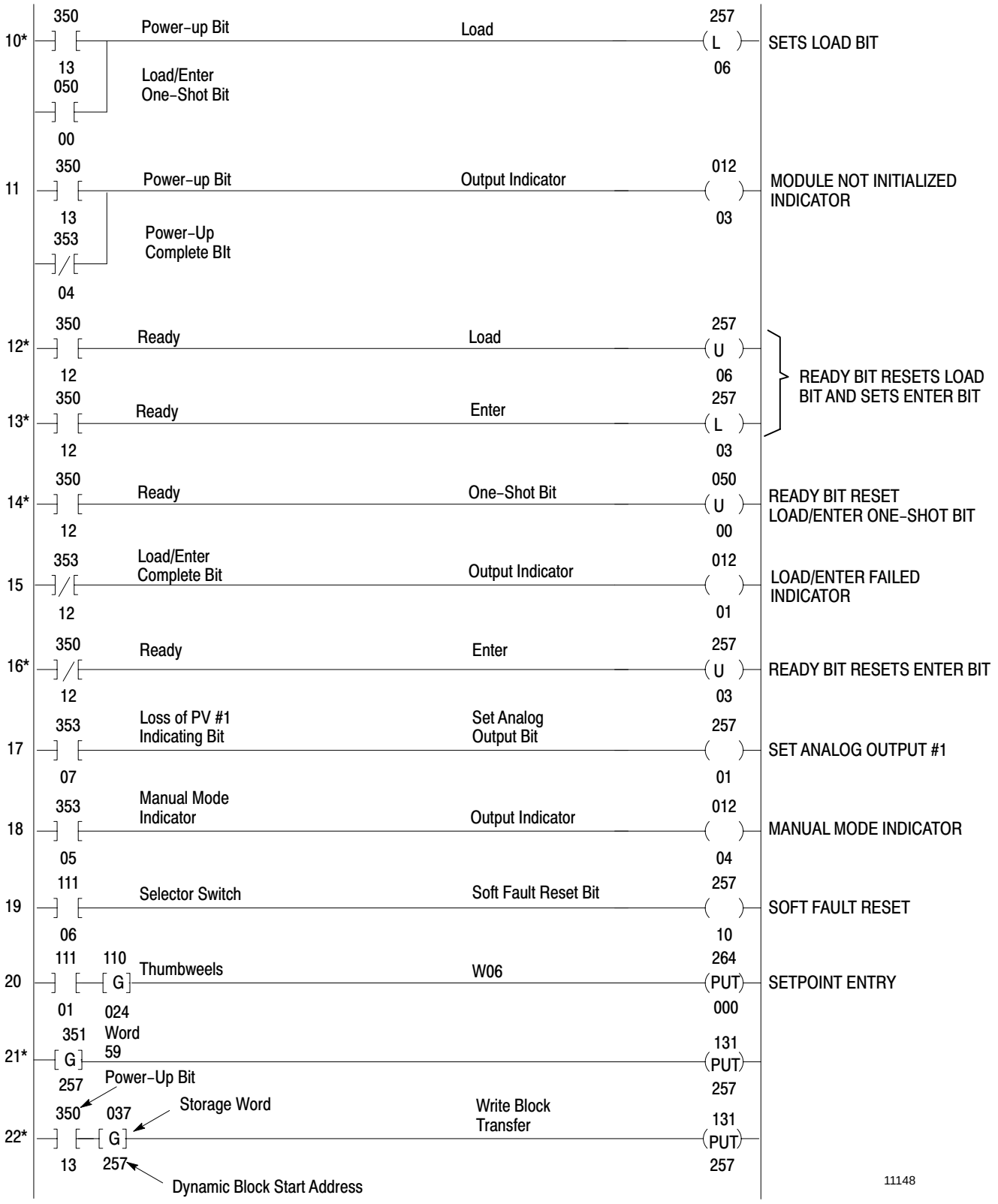
The ladder diagram program for PLC-2 family processors that use block format instructions is presented on the next three pages.

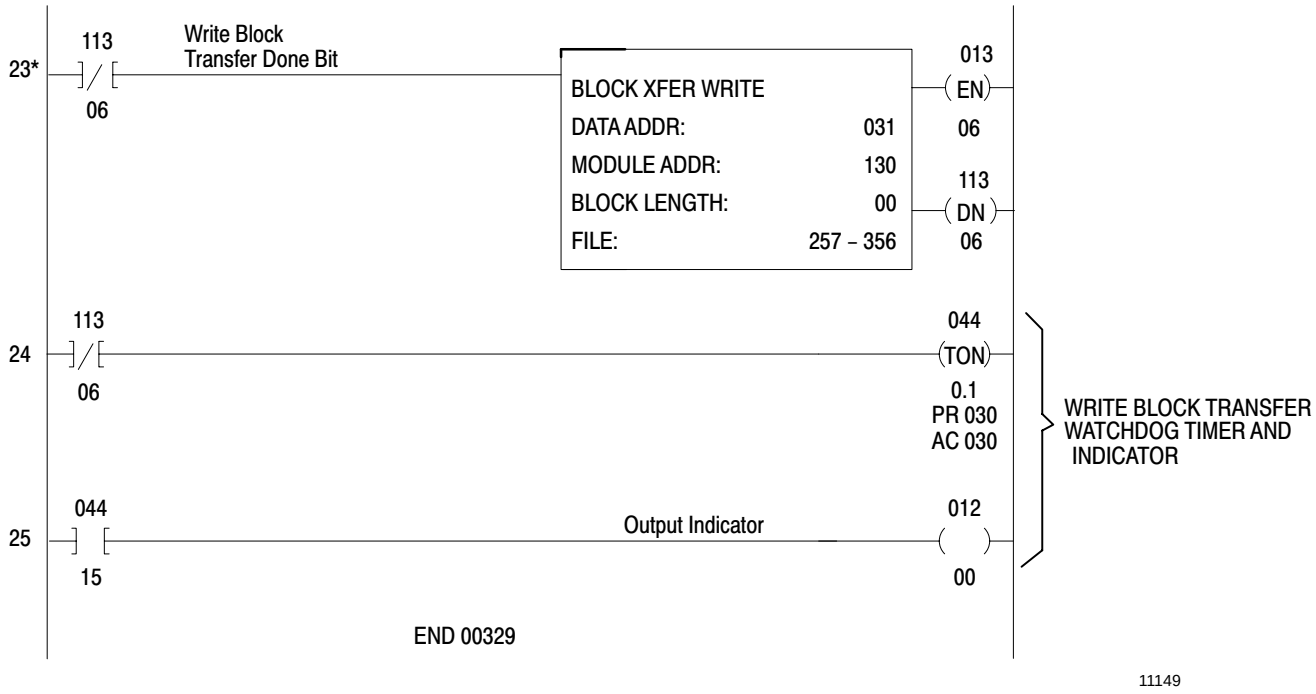
Figure B.2
Ladder Diagram Program, Example 1



*minimum required rungs to program the module

11147


10*
350
Power-up Bit
Load
257
L
06
SETS LOAD BIT
13
050
Load/Enter
One-Shot Bit
00
11
350
Power-up Bit
Output Indicator
012
03
MODULE NOT INITIALIZED INDICATOR
13
353
Power-Up
Complete BIt
04
12*
350
Ready
Load
257
U
06
READY BIT RESETS LOAD BIT AND SETS ENTER BIT
12
13*
350
Ready
Enter
257
L
03
12
14*
350
Ready
One-Shot Bit
050
U
00
READY BIT RESET LOAD/ENTER ONE-SHOT BIT
12
15
353
Load/Enter
Complete Bit
Output Indicator
012
01
LOAD/ENTER FAILED INDICATOR
12
16*
350
Ready
Enter
257
U
03
READY BIT RESETS ENTER BIT
12
17
353
Loss of PV #1
Indicating Bit
Set Analog
Output Bit
257
01
SET ANALOG OUTPUT #1
07
18
353
Manual Mode
Indicator
Output Indicator
012
04
MANUAL MODE INDICATOR
05
19
111
Selector Switch
Soft Fault Reset Bit
257
10
SOFT FAULT RESET
06
20
111
110
G
Thumbweels
W06
264
PUT
000
SETPOINT ENTRY
01
024
21*
351
G
Word
59
131
PUT
257
Power-Up Bit
257
22*
350
037
G
Storage Word
Write Block
Transfer
131
PUT
13
257
257
Dynamic Block Start Address
11148



Program Rung Descriptions

rung 1* Display run. It allows the words pertaining to the module's operating characteristics and parameters to be monitored or changed using the data monitor mode of the industrial terminal. Because the words are stored in consecutive files, the position numbers in the data monitor mode will match the module word numbers.

rungs 2 thru 4* When pushbutton 111/00 is closed, storage bit 050/00 is latched. This bit is subsequently used in rung 10 to latch the load bit and initialize a load/enter sequence. A load/enter sequence can be initiated at any time. Bit 050/00 is unlatched in rung 14 by the ready bit.

rung 5* Zeros are loaded into timer/counter address 032 8. The boundary tells the processor not to look beyond word 0328 for data addresses associated with block transfer instructions.

rung 6* The read block transfer instruction reads the next status block of data set by the module and transfers it to the input

buffer area of the data table (words 233-2548). The rung is conditioned by the read block transfer done bit 113/07.

When the block length is set to the default value, 00, the instruction automatically displays a file length of 64 words (words 233-3328). However, the PID module will only transfer 18 words in a read block transfer. The remaining 46 words can be used for other purposes such as timers, counters and word bit storage.

rung 7* Upon completion of a valid read block transfer determined by examining the block transfer done bit 113/07, the data from the buffer area is transferred to the status area of the data table (words 347-3708). Indentifier bits 16 and 17 of word 2348 are examined for an off condition to ensure that the data residing in the buffer area is indeed that of the status block.

rung 8* Timer 0438 is the read block transfer watchdog timer. It begins timing whenever the read block transfer done bit 113/17 is low. Upon completion of a valid read block transfer, the done bit goes high and resets the timer. The preset value of this timer is user-selectable.

rung 9 Annunciator lamp 012/02 illuminated when the read block transfer watchdog timer times out.

rung 10* The load bit 257/06 is latched when either the power-up bit 350/13 or store bit 050/00 is high. (Refer to explanation for rungs 2 thru 4.) When latched, 257/06 initiates a load/enter sequence.

rung 11 The MODULE NOT INITIALIZED indicator 012/03 illuminates when the power-up bit 350/13 is high or the power-up complete bit 353/04 is low.

rung 12* When energized, the ready bit 350/12 sets the enter bit 257/06.

rung 13* When energized, the ready bit 350/12 sets the enter bit 257/03.

rung 14* When energized, the ready bit resets load/enter one-shot bit 050/00.

rung 15 The indicator 012/01 illuminates when the load/enter complete bit 353/12 is low.

rung 16* The enter bit 257/03 is reset when the ready bit 350/12 goes low.

rung 17 Bit 353/07 goes high upon loss of signal at analog input 1. This in turn sets 257/01 high allowing the analog output to go to a user programmed value stored in word 2638, module word W05.

rung 18 Annunicator lamp 012/04 illuminates, via the manual mode indicating bit 353/05, when the manual control station is in the manual mode.

rung 19 When selector switch 111/06 is closed, the soft fault reset bit 257/10, module bit W01 B10, is set.

rung 20 A 4-Digit BCD value residing in data table location 1108 is loaded into the setpoint word of the dynamic block when pushbutton 111/01 is closed. This rung facilitates user enter of setpoint values.

NOTE: Although the get/put statement displays only the values of the first 12 bits in word 1108, it functionally transfers all 16 bits into word 2548.

rung 21* This rung loads the location of the next data block requested by the module (next block start address) into the block transfer write instruction.

rung 22* If the power-up bit 350/13 is set, the get instruction fetches the dynamic block start address stored in word 0378. the put instruction places the dynamic block start address in the block transfer write instruction word 1318 (1008 above data address). This rung will be true only until the first load/enter sequence is executed. When true, it will override rung 21.

rung 23* The block transfer write instruction will write block data from the file location loaded into word 1318 to the module (the file location is determined by rungs 21 and 22). This instruction is conditioned by the write block transfer done bit.

rung 24 Timer 0448 is the write block transfer watchdog timer. It will increment whenever the write block transfer done bit 113/06 is low. Upon completion of a valid write block transfer, the done bit goes high and resets the timer. The preset of this timer is user-selectable.

rung 25 Annunicator lamp 012/00 will illuminate when the write block transfer watchdog timer times out.

*minimum required rungs to program the module

Descriptive Figures and Tables

Refer to the following figures and tables which describe the PLC-2 family program:

- data table information showing the storage and instruction address (Table B.A)
- functional bit/word addresses and descriptions (Table B.B)
- data table map showing the dynamic block, loop blocks and status block locations (NO TAG)
- recommended output annunciators, (Table B.C)

Table B.A
Data Table Information

Word Address	Number of Words
Input Buffer Location words 233_8-256_8	20
Dynamic Block Location words 257_8-277_8	17
Loop 1 Block Location words 300_8 -322_8	19
Loop 2 Block Location words 324_8 -346_8 (available for other storage)	
Status Block Location words 347_8 - 370_8	18
Timers/Counters 043_8 , 044_8, 143_8 , 144_8	4
Block Transfer Instructions 030_8 , 031_8, 130_8 , 131_8	4
File-To-File Move Instructions 040_8 , 041_8 , 140_8 , 141_8	4
Storage Words 032_8 , 033_8 , 037_8 , 050_8	4
Total	90
Pushbutton/Selector Switches PB 111/00, PB 111/01, SS 111/06	
Output Indicators 012/00, 012/01, 012/02, 01203, 012/04	
Storage Bits 050/00, 050/01	
Module Location rack 1, module group 3: 113 input image table, 013 output image table	
PC Processor Type PLC-2/30	
Ladder Diagram Program Length 73 words	

Table B.B
Functional Bit/Word Descriptions

PROGRAM ADDRESS	MODULE ADDRESS [1]		FUNCTION
257/01	W01	B01	When set, allows a programmed value to be downloaded to analog output 1.
275/03	W01	B03	Enter bit
257/06	W01	B06	Load bit
350/12	W58	B12	Ready bit
353/04	W61	B04	Power-up bit
353/05	W61	B05	Set when manual control station is in the manual mode.
353/07	W61	B07	Set when analog input 1 has gone below minimum.
353/12	W61	B12	Load/enter complete bit
263_8	W05		Analog output 1 download from the PC processor.
264_8	W06		Loop 1 setpoint
351_8	W59		Contains data table location of the next data block required by the module.

[1] W01 master control word (dynamic block)
W05 word for set analog output 1 (dynamic block)
W06 set point word (dynamic block)
W58 alarm word (status block)
W59 word for next block start address (status block)
W61 status word (status block)

Figure B.3
Data Table Map
Allen-Bradley Programmable Controller
Data Table MAP (128-word)
(Publication 5045 - February, 1982)

PAGE____ OF ____
ADDRESS____ TO ____

PROJECT NAME Example 1 Program
PROCESSOR PLC-2/30
DESIGNER
DATA TABLE SIZE 540

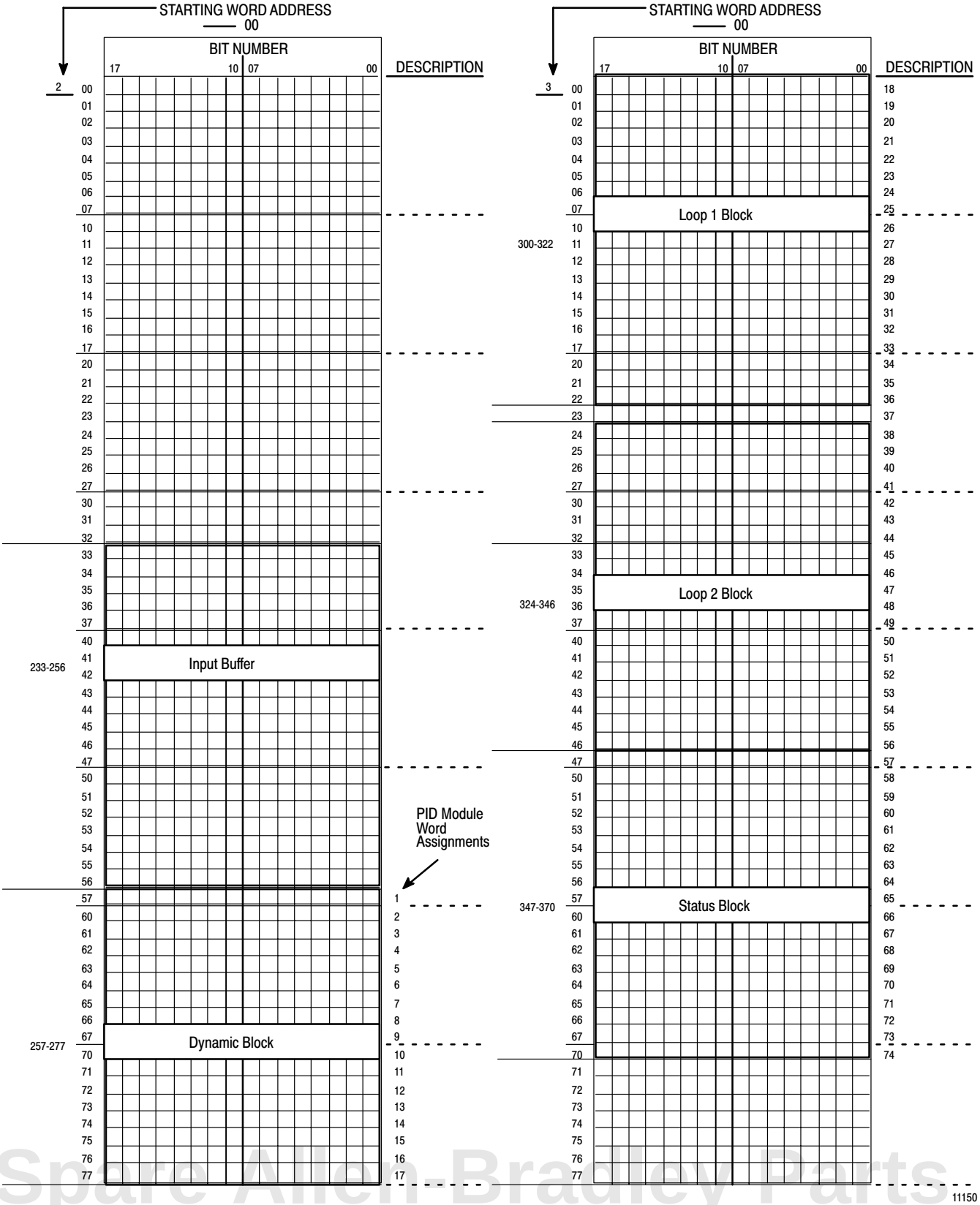


Table B.C
Recommended Output Annunicators

DESCRIPTION	FUNCTION
BLOCK TRANSFER WATCHDOG Indicators Program Address 012/01-READ 012/00-WRITE	These indicators illuminate if a read or write block transfer does not occur within a predetermined time. The time is determined by the preset value selected for timer instructions 043_8 or 044_8 will time-out and energize indicators 012/02 or 012/00 depending upon whether the read or write function failed (rungs 9 and 25)
MANUAL MODE Indicator Program Address 012/04	This indicator illuminates when the manual control station (if used) is in the manual mode (rung 18).
MODULE NOT INITIALIZED Indicator Program Address 012/03	This indicator illuminates when the module has just been powered and is waiting for operating parameters from the processor. The indicator turns off after the first successful load/enter sequence (rung 11).

Specific Example

Once the program has been written, specific data of the dynamic block and loop block can be entered into the respective data table files. This can be done using the data monitor display mode of the industrial terminal. Place the cursor on the file-to-file move instruction in rung 1 and press the (DISPLAY)(1) Keys on the industrial terminal keyboard. The hexadecimal display of the dynamic block and loop blocks will appear on the screen. Enter the selected standard and expanded feature values. On-line data change (SEARS)(5)(1) can be used.

The features and values that have been selected for this example problem are tabulated below according to the control word in which the features are programmed.

Master Control Word W01

Bits 17, 16 = 1	Both identifier bits must be 1.
Bit 15 = 1	Loop 1 only is selected.
Bit 14 = 0	Expanded features are not used.
Bit 13 = 0	Calibration bit must be 0.
Bit 12 = 0	Format is BCD.
Bit 11 = 0	Setpoint format is BCD.
Bit 10 = 0	Soft fault is programmed for manual reset.

	Bit 10 is controlled in rung 19
Bit 07 = 0	Loop time is reported in the status monitor byte.
Bit 06	Load bit is controlled by user program.
Bit 05, 04	Verify bits must be 0.
Bit 03 = 0	Enter bit is controlled by user program.
Bit 02 = 0	Set output bit is not used.
Bit 01 = 0	Analog output is set to programmed value if loss of PV input occurs. Bit 01 is controlled in rung 17.
Bit 00 = 0	Manual request bit is not used.

Loop 1 Control Word A W18

Bit 17 = 0	Block identifier must be 0.
Bit 16 = 1	Block identifier must be 1.
Bit 15 = 0	The source of the process variable input is the analog input.
Bit 14 = 0	Square root is not used.
Bit 13 = 0	Error is positive (SP-PV).
Bit 12 = 0	Error limiting is not used.
Bit 11 = 1	Dead band is set to 15 in word W23.
Bit 10 = 1	Integral output is limited to 4000 in word W26.
Bits 07,06 = 0	Proportional error is not modified.
Bits 05,04 = 0	Integral error is not modified.
Bit 03 = 0	Derivative error is not modified.
Bit 02 = 0	Derivative output is not limited.
Bit 01 = 0	PID output is not held.
Bit 00 = 0	Bias is not held.

Loop 1 Control Word B W19

Bit 17 - 0	Bias is added to the output.
Bit 16 = 1	Output is limited to 4050 in word W29.
Bit 15 = 1	Soft fault response is to continue PID control.
Bit 14 = 0	Soft fault response is to continue PID control.
Bit 13 = 0	Soft fault response is to continue PID control
Bit 12 = 0	Digital filter time is multiplied x1.
Bit 11 = 0	Lead time constant TB is multiplied x1
Bit 10 = 0	Lag time constant TC is multiplied x1

Bit 07 = 0	Scaled Set Point value is positive
Bit 06= 0	Scaling Word is multiplied x1
Bits 05,04 = 0	K_P multiplier is x1.
Bits 03,02 = 0	K_I multiplier is x1.
Bits 01,00 = 0	K_D multiplier is x1.

Selected feature values for this example program have been recorded in Worksheets 1 and 2 (NO TAG and Figure B.5, respectively). Worksheet 1 shows the dynamic block (data table words 257-277$_8$). The PID module word numbers correspond to the position numbers on the display and are numbered W01 through W17. Worksheet 2 shows the loop 1 block (data table words 300-322$_8$). The PID word numbers (position numbers) are W18 through W36. Also refer to the data table map (NO TAG) which shows the locations of the consecutive data blocks.

Figure B.4

Allen-Bradley Programmable Controller
1771-PD Module Worksheet 1
Dynamic Block

Page 1 of 2

Project Name: Example Program Processor: PLC-2/30
Designer: _____ Data Table Size: 640

DATA TABLE WORD USAGE From 257 to 277

Data Table Word Address	Module Word #	Name	Value	Range	BCD or BIN	Multiplier	Sign
	[3]		17 14 13 10 07 04 03 00				
257	W01	Master Control Word	1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	FFFF	→	E000 [4]	
260	W02	Control Word		F000	--		
261	W03	Dynamic Block Start Address	0 | 2 | 5 | 07	FFFF	--		
262	W04	Loop 1 Block Start Address	0 | 3 | 0 | 00	FFFF	--		
263	W05	Set Analog Output 1 SET OUT1	2 | 0 | 4 | 28	4095	[1]		
264	W06	Set Point 1 SP1	3 | 0 | 7 | 32	4095/ 9999	[2]	x!0 W19B06 (+) [5]	W19 B07– (+)
265	W07	Proportional Gain 1 K_P1	4 | 5 | 5 | 40	99.99	--	W19 B05,04 x1 [6]	
266	W08	Bias 1 BIAS1	0 | 0 | 9 | 06	9999	--		
267	W09	Set Process Variable 1 SET PV1	0 | 0 | 0 | 00	4095	[1]		
270	W10	Set Feedforward Input 1 SET FFI1	0 | 0 | 0 | 00	4095	[1]		
271	W11	Loop 2 Block Start Address	0 | 0 | 0 | 00	FFFF	--		

272	W12	Set Analog Output 2 SET OUT2	0 | 0 | 0 | 0	4095	[1]		
273	W13	Set Point 2 SP2	0 | 0 | 0 | 0	4095/ 9999	[2]	x10 W39 B06 (x1)	W39 B07- [5] (+)
274	W14	Proportional Gain 2 K_P2	0 | 0 | 0 | 0	99.99	--	W39 B05, 04 x1	[6]
275	W15	Bias 2 BIAS2	0 | 0 | 0 | 0	9999	--		
276	W16	Set Process Variable 2 SET PV2	0 | 0 | 0 | 0	4095	[1]		
277	W17	Set Feedforward Input 2 SET FFI2	0 | 0 | 0 | 0	4095	[1]		

NOTES:
For the BCD or Binary column:
[1] denotes selection by W 01 B12
[2] denotes selection by W 01 B11
[3] also represents the displayed position number
[4] record Hex value
[5] circle choice
[6] record value

Figure B.5
Worksheet 2 for Loop 1 Block

Allen-Bradley Programmable Controller
1771-PD Module Worksheet 2
Loop 1 Block

Page 2 of 2

Project Name: Example Program Processor: PLC-2/30

Designer: _____ Data Table Size: 540

DATA TABLE WORD USAGE From 300 to 322

Data Table Word Address	Module Word #	Name	Value	Range	BCD or BIN	Multiplier	Sign
	1		17 14 13 10 07 04 03 00				
300	W18	Loop 1 Control Word A	0 1 0 0 0 0 1 1 0 0 0 0 0 0 0 0	FFFF	→	4300 (2)	
301	W19	Loop 1 Control Word B	0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	FFFF	→	6000 (2)	
302	W20	Input Filter Time Constant 1 TA1	0 | 1 | 9 | 0	99.99	--	x10 W19 B12 (x1)	3
303	W21	Maximum Negative Error 1 EMN1	4 | 0 | 9 | 5	4095	--		
304	W22	Maximum Positive Error 1 EMP1	4 | 0 | 9 | 5	4095	--		
305	W23	Dead Band 1 DB1	0 | 0 | 1 | 5	4095	--		
306	W24	Integral Gain 1 K_I1	0 | 6 | 0 | 0	9.999	--	W19 B03,02 x1	4
307	W25	Derivative Gain 1 K_D1	0 | 0 | 0 | 0	99.99	--	W19 B01,00	4
310	W26	Integral Term Limit 1 V_IMAX1	4 | 0 | 0 | 0	9999	--		
311	W27	Derivative Term Limit 1 V_DMAX1	4 | 0 | 9 | 5	9999	--		
312	W28	Minimum Output Limit 1 VMIN1	0 | 0 | 0 | 0	4095	--		

313	W29	Maximum Output Limit 1 VMAX1	4 | 0 | 9 | 5	4095	--		
			17 14 | 13 10 | 07 04 | 03 00				
314	W30	Loop 1 Expanded Control Word	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	FFFF	→		
315	W31	Minimum Scaling Value 1 SMIN1	0 | 0 | 0 | 0	9999	--		W30 B04 - + [3]
316	W32	Maximum Scaling Value 1 SMAX1	0 | 0 | 0 | 0	9999	--		W30 B03 - + [3]
317	W33	Feedforward Offset 1 FFO1	0 | 0 | 0 | 0	9999	--		
320	W34	Feedforward Gain 1 K_F1	0 | 0 | 0 | 0	99.99	--	W30 B07,06	[4]
321	W35	Lead Time Constant 1 TB1	0 | 0 | 0 | 0	99.99	--	W19 B11 x10 x1	[3]
322	W36	Lag Time Constant 1 TC1	0 | 0 | 0 | 0	99.99	--	W19 B11 x10 x1	[3]

NOTES:
[1] also represents the displayed position number
[2] record Hex value
[3] circle choice
[4] record value

Program PLC-3 Processors

The PLC-3 program for continuous block transfer is presented in figure B.6 Worksheets for the Dynamic block (figure B.4) and Loop 1 Block (Figure B.5) also apply to the PLC-3 program. File storage addresses are tested in Table B.D.

Table B.D
PLC-3 File Storage Addresses
(shown in hex)

Start = WB000:0000

Word number	0	1	2	3	4	5	6	7
00000	**0001**	**E180**	0000	**0001**	**0012**	0000	**3303**	**0050**
00008	0000	0000	0000	**0026**	0000	0000	0000	0000
000116	0000	0000	**4000**	0000	0000	0000	**4095**	0000
00024	0000	0000	0000	0000	0000	**4095**	0000	0000
00032	0000	0000	0000	0000	0000	0000	**8000**	0000
00040	0000	0000	0000	0000	0000	0000	0000	0000
00048	0000	0000	0000	0000	0000	0000	0000	0000
00056	0000	0000	0000	**0001**	0000	**0450**	**2203**	**1101**
00064	**1100**	**1100**	0000	0000	0000	0000	0000	0000
00072	0000	0000	0000	0000	0000	0000	0000	0000

Dynamic Block - binary file 0, words 1 thru 17

start location: 00000000 00000001 in binary, 0001 in hex

Loop 1 Block - binary file 0, words 18 thru 36

start location: 00000000 00010010 in binary, 0012 in hex

Loop 2 Block - binary file 0, words 38 thru 56

start location: 00000000 00100110 in binary, 0026 in hex

Status Block - binary file 0, word 57 thru 74

Input Buffer - binary file 2, words 0 thru 20

Block Transfer Control File - Binary file 3

Module Location: rack 2, module group 1

NOTE: Block transfer control file must be the same for the read and write block transfer instructions.

Binary file 0 word 0 is used to store the dynamic block start address (rung l3 in the continuous block transfer program, rung 23 in the periodic block transfer program).

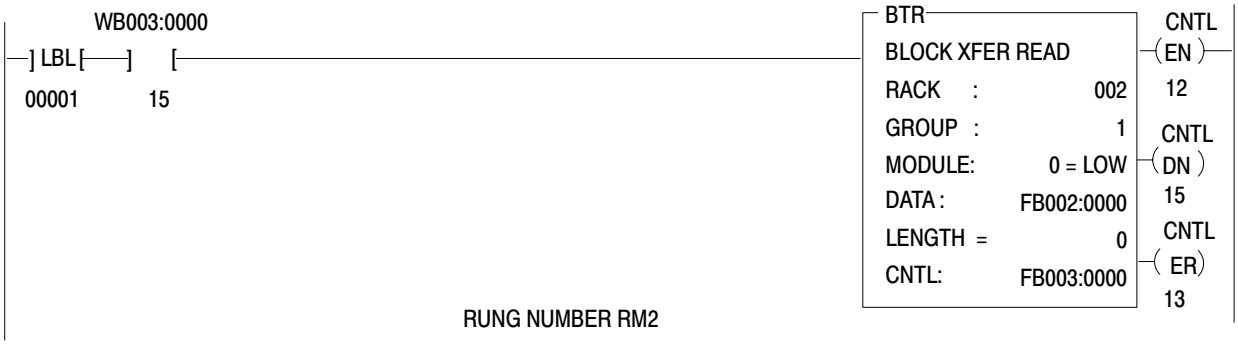
Figure B.6
PLC-3 Continuous Block Transfer Program

RUNG NUMBER RM0

THIS RUNG ENERGIZES T1/16 FOR ONE CPU SCAN WHEN PUSHBUTTON 012/00 IS CLOSED. THIS BIT THEN SETS THE "LOAD" BIT IN RM5 TO INITIATE A LOAD/ENTER SEQUENCE

RUNG NUMBER RM1

PERFORMS A "READ" OF THE STATUS BLOCK FROM THE -PD MODULE AND TRANSFERS THAT BLOCK INTO A USER-SPECIFIED BUFFER AREA. (*NOTE*-BLOCK TRANSFER RUNG MUST BE CONDITIONED WITH AN "XIO" OF ITS' RESPECTIVE "DONE" BIT)



RUNG NUMBER RM2

UPON COMPLETION OF A SUCCESSFUL "READ" OF THE STATUS BLOCK INTO THE BUFFER AREA, (SIGNIFIED BY AN "ON" CONDITION OF THE READ BLOCK TRANSFER "DONE" BIT) THE STATUS BLOCK IS MOVED FROM THE BUFFER TO THE USER SPECIFIED STATUS AREA.

RUNG NUMBER RM3

READ BLOCK TRANSFER "WATCHDOG" TIMER, SHOULD A SUCCESSFUL READ BLOCK TRANSFER NOT OCCUR WITHIN THE USER PRESET TIME, THE TIMER WILL "TIME-OUT" TO INDICATE A READ BLOCK TRANSFER FAILURE, (*NOTE*-RUNG IS CONDITIONED BY AN "XIO" OF THE READ BLOCK TRANSFER "DONE" BIT).

RUNG NUMBER RM4

OUTPUT ANNUNICATOR 0013/00 WILL ENERGIZE TO INDICATE A READ BLOCK TRANSFER FAILURE

RUNG NUMBER RM5

THIS RUNG INITIATES A LOAD/ENTER SEQUENCE AUTOMATICALLY AT POWER-UP AND ALSO AT THE USER'S DISCRETION. RUNG IS CONDITIONED BY THE "POWER-UP" BIT AND BY THE USER CONTROLLED ONE-SHOT BIT, ANYTIME THE "LOAD" BIT IS SET, A LOAD/ENTER SEQUENCE IS EXECUTED.

RUNG NUMBER RM6

OUTPUT ANNUNCIATOR 013/01 WILL ENERGIZE TO INDICATE THE -PD MODULE IS NOT INITIALIZED, THE RUNG IS CONDITIONED BY THE "POWER-UP" BIT AND THE "POWER-UP COMPLETE" BIT.

RUNG NUMBER RM7

DURING A LOAD/ENTER, SEQUENCE, THE "READY" BIT WILL SET THE "ENTER" BIT AND RESET THE "LOAD" BIT.

RUNG NUMBER RM8

OUTPUT ANNUNCIATOR 013/02 WILL ENERGIZE BRIEFLY DURING THE EXECUTION OF A LOAD/ENTER SEQUENCE. SHOULD IT REMAIN ENERGIZED, THE LOAD/ENTER SEQUENCE WAS NOT SUCCESSFULLY COMPLETED.

RUNG NUMBER RM9

UPON SUCCESSFUL COMPLETION OF THE LOAD/ENTER SEQUENCE, THE "READY' BIT RESETS THE"ENTER" BIT.

RUNG NUMBER RM10

THIS RUNG AFFORDS THE USER MANUAL CONTROL OVER THE “SOFT–FAULT RESET” BIT VIA SELECTOR SWITCH 12/10

RUNG NUMBER RM11

VALUES FROM THUMBWHEELS (REGISTER “A”) ARE MOVED INTO THE SETPOINT WORD WHEN PUSHBUTTON 12/01 IS CLOSED.

RUNG NUMBER RM12

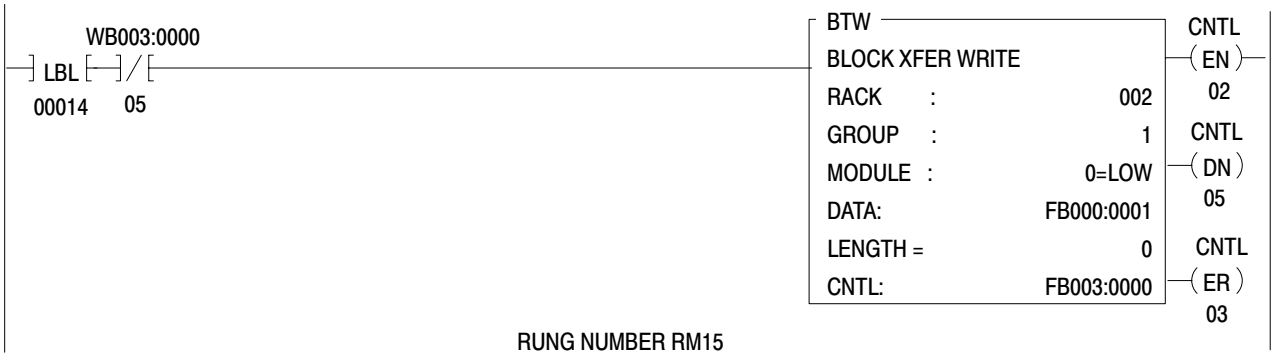
THIS RUNG MOVES THE DATA TABLE ADDRESS OF THE NEXT BLOCK OF PARAMETERS REQUESTED BY THE -PD MODULE INTO THE 4TH WORD OF THE BLOCK TRANSFER CONTROL FILE. THIS ALLOWS THE BLOCK TRANSFER WRITE INSTRUCTION TO SEND THE CORRECT FILE TO THE MODULE.

RUNG NUMBER RM13

AT POWER-UP, THE DATA TABLE ADDRESS OF THE STARTING LOCATION OF THE DYNAMIC BLOCK (REGISTER "A" IN "MOV" INSTRUCTION) IS MOVED INTO THE 4TH WORD OF THE BLOCK TRANSFER CONTROL FILE. THIS RUNG IS EXECUTED ONLY WHILE THE MODULE IS IN THE POWER-UP MODE AND IS OVERRIDDEN BY RM12 THEREAFTER.

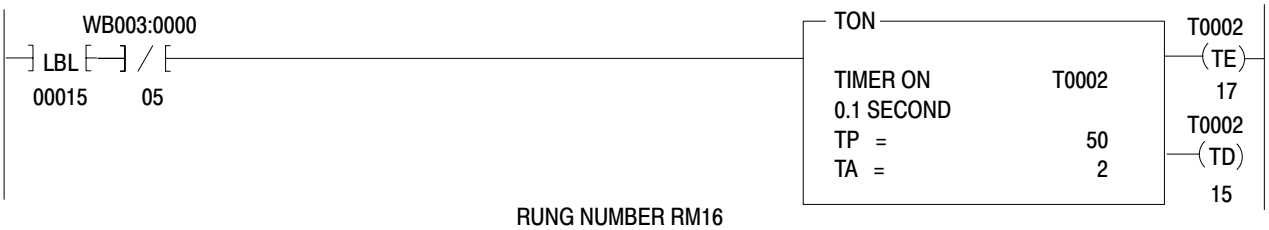
RUNG NUMBER RM14

THIE RUNG WRITES EITHER THE DYNAMIC OR THE LOOP BLOCKS TO THE -PD MODULE AS DICTATED BY RUNGS RM12 AND RM13, (*NOTE*-BLOCK TRANSFER RUNGS MUST BE CONDITIONED BY AN "XIO" OF THEIR RESPECTIVE "DONE" BITS)



RUNG NUMBER RM15

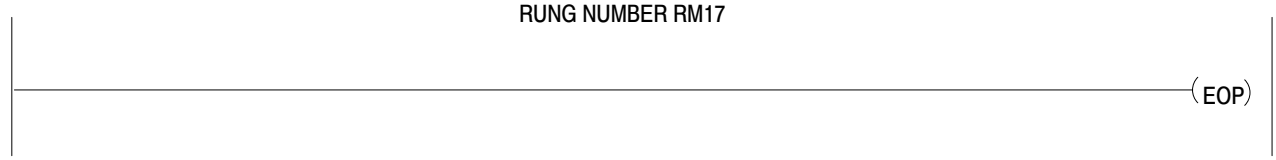
WRITE BLOCK TRANSFER "WATCHDOG" TIMER. SHOULD A SUCCESSFUL WRITE BLOCK TRANSFER NOT OCCUR WITHIN THE USER SPECIFIED PRESET TIME, THE TIMER WILL "TIME-OUT" INDICATING A WRITE BLOCK TRANSFER FAILURE, (*NOTE*-RUNG IS CONDITIONED BY AN "XIO" OF THE WRITE BLOCK TRANSFER "DONE" BIT)



RUNG NUMBER RM16

OUTPUT ANNUNCIATOR 013/04 WILL ENERGIZE TO INDICATE A WRITE BLOCK TRANSFER FAILURE

RUNG NUMBER RM17



Appendix C

Application Example 2, Periodic Block Transfer

General

The periodic block transfer program allows you to keep the number of PID block transfers to a minimum, so as not to increase the block transfer times of other block transfer modules in the system. The example described in this appendix is a 2-loop application that could use continuous or periodic block transfer programming. The first loop controls temperature, the second controls flow. Both loops operate independently.

Following the program description, typical values of selected standard and expanded control features are introduced using a worksheet for each dynamic block and loop block. Worksheets simplify record keeping associated with programming the module. Worksheet forms in appendix A should be reproduced and used as needed.

Example Application

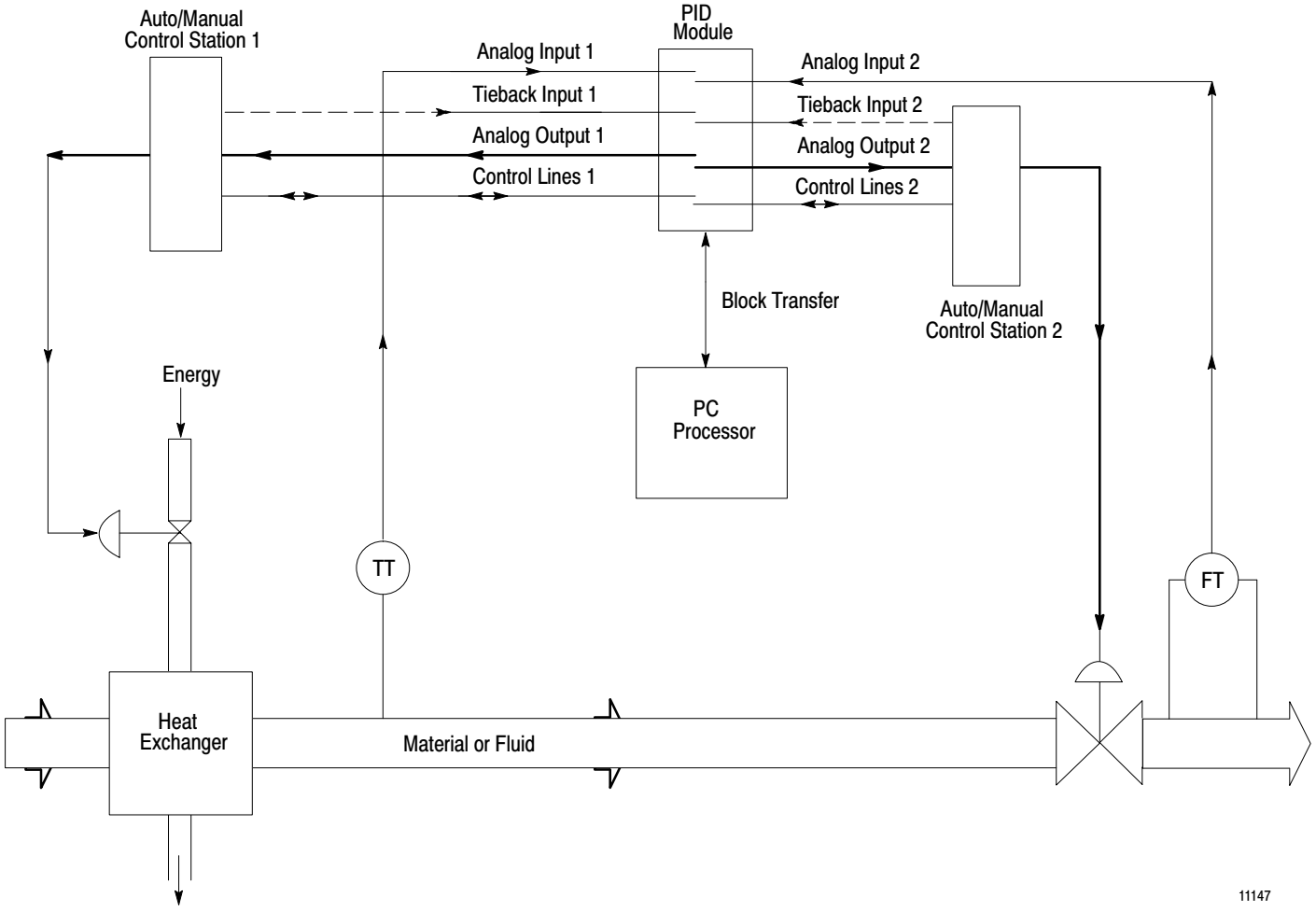
A fluid or material is passed through a heat exchanger where the temperature is maintained at a setpoint for loop 1 and then through a valve where the flow is maintained at a flow setpoint for loop 2. A temperature transducer monitors the temperature of the fluid or material as it exits the heat exchanger in loop 1. A flow transducer monitors the flow rate as the fluid or material leaves the flow control value in loop 2. The output of loop 1 controls the energy permitted into the heat exchanger while the output of loop 2 regulates the rate of flow of material or fluid. A manual control station is electrically connected in each loop to provide manual back-up if needed (Figure C.1).

Program for PLC-2 Family Processors

This example program shows the PID module's stand alone operation feature where operating parameters are transferred to the module during an initial load/enter sequence. Thereafter, block transfers are minimized. The status monitor byte reports module status when block transfer instructions are not enabled. Periodically, a read block transfer and watchdog timer instruction are enabled to verify communication with the PID module. A parameter change, whether to the dynamic block or loop blocks, requires a manually initiated load/enter sequence. It can be initiated by an operator at any time.

In this program example, there are four circumstances when a load/enter sequence must be initiated. In two circumstances, the load/enter sequence is initiated automatically by user program. In the other two, the sequence is initiated manually.

Figure C.1
2-Loop Temperature/Flow Control



The circumstances in which the load/enter sequence is program initiated are:

1. Processor Power-Up: On the first scan of user program, program logic will initiate a load/enter sequence. This is true for powering up the PC processor in the run mode and when PC processor operation is changed from program or test mode to run mode.

2. Alarm Condition at Module: Should a condition occur at the module which causes any of the diagnostic bits in the status monitor byte to be set, the user program will automatically begin to execute continuous load/enter sequences until the alarm condition is corrected. This will allow an operator to observe the source of error in diagnostic word W60 and to manually enter commands to clear the fault. Once the alarm condition is corrected, the program will stop executing load/enter sequences and return to its original operating state.

If the following limiting functions are not used, enter the maximum value from the table to prevent the processor from initiating nuisance load/enter sequences.

Limit	Word	Max Value
EMN	W21(W41)	-4095
EMP	W22(42)	+4095
V_IMAX	W26(W46)	9999
V_DMAX	W27(W47)	9999
V_DMIN	W28(W48)	0000
VMAX	W29(W49)	4095

The circumstances in which the load/enter sequence is initiated manually are:

1. Pushbutton Initiated: A load/enter sequence can be executed manually at any time. An example would be changing the loop gain constants. The program examines the contacts of a pushbutton switch. When the contacts close, one load/enter sequence will be executed. To execute another sequence, the contract must open and close again.

NOTE: The pushbutton contact can be substituted with bit 15 from a free-running timer allowing a load/enter sequence to be executed periodically.

2. Setting the Soft Fault Reset Bit: When communication between the PID module and processor has been interrupted (such as a disconnected or broken I/O inteconnect cable) the module will enter the soft fault mode of operation. After the condition which caused the fault is corrected, either one of two possible module responses will occur depending on the state of the soft fault reset bit W01 B10.

a. W01 B10 = 1 The module will enter the normal operating mode immediately after the condition is corrected.

b. W01 B01 = 0 The module will remain in soft fault mode.

If the latter condition exists, the program will be attempting load/enter sequences because bit 00 of the status monitor byte is high. The module will not allow a load/enter sequence to occur until bit 257/10, corresponding to module bit W01 B10, is set in the program by selector switch 111/06. When set, the module will enter the normal operating mode and load/enter sequence will be executed. This feature allows the operator to decide when the module will enter the normal operating mode after a soft fault condition has been corrected. The operator may wish to determine the cause of the soft fault and determine current status before returning control to the PID module.

The program also allows the analog output to be set to a programmed value in the event of a lost of the process variable signal. If the PV signal at analog input 1 should become lost, the module would normally hold the last analog output value. This program examines the loss of input bit W61 B07 and sets the bit in the master control word which allows the value in word W05 to determine the analog output.

When the PV signal is restored, the module automatically returns to normal operation where the analog output is determined by the PID algorithm.

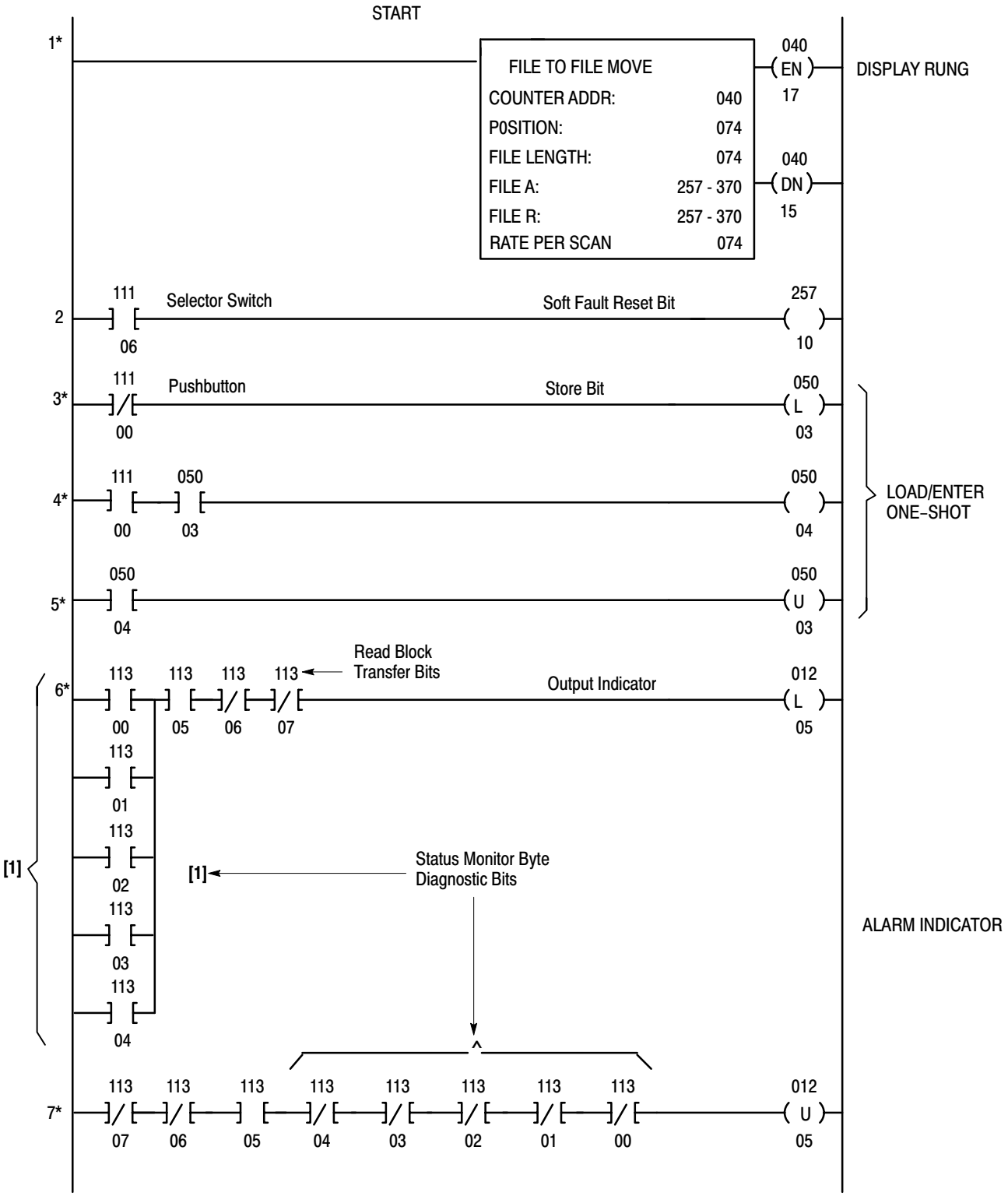
Also incorporated in the program is a provision which causes a read block transfer to occur periodically at a user-defined time interval. This allows loop status parameters to be reported to the PC processor as a safe-guard to ensure that the system is operating correctly.

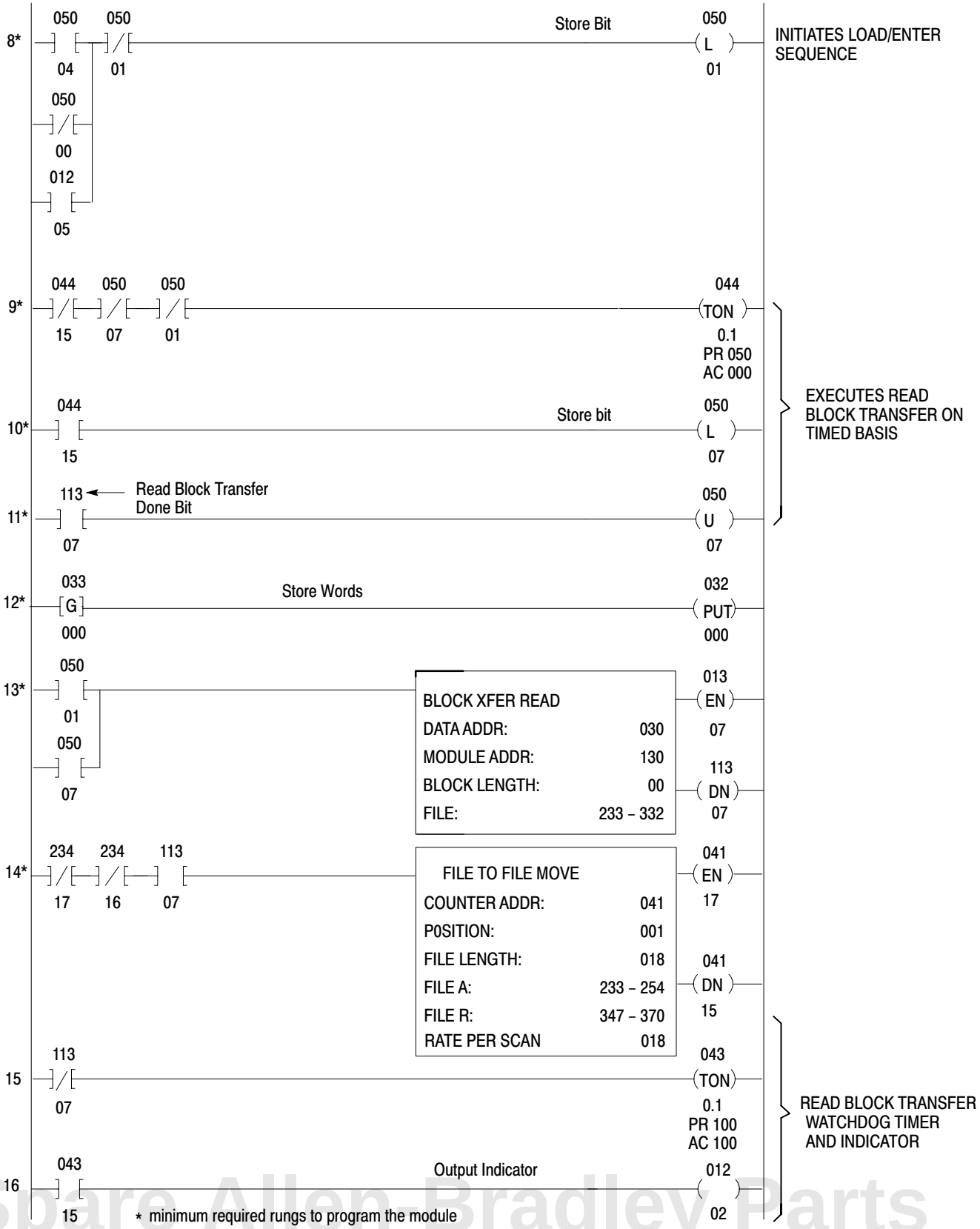
Indicators have been programmed to illuminate if any of the following conditions should occur:

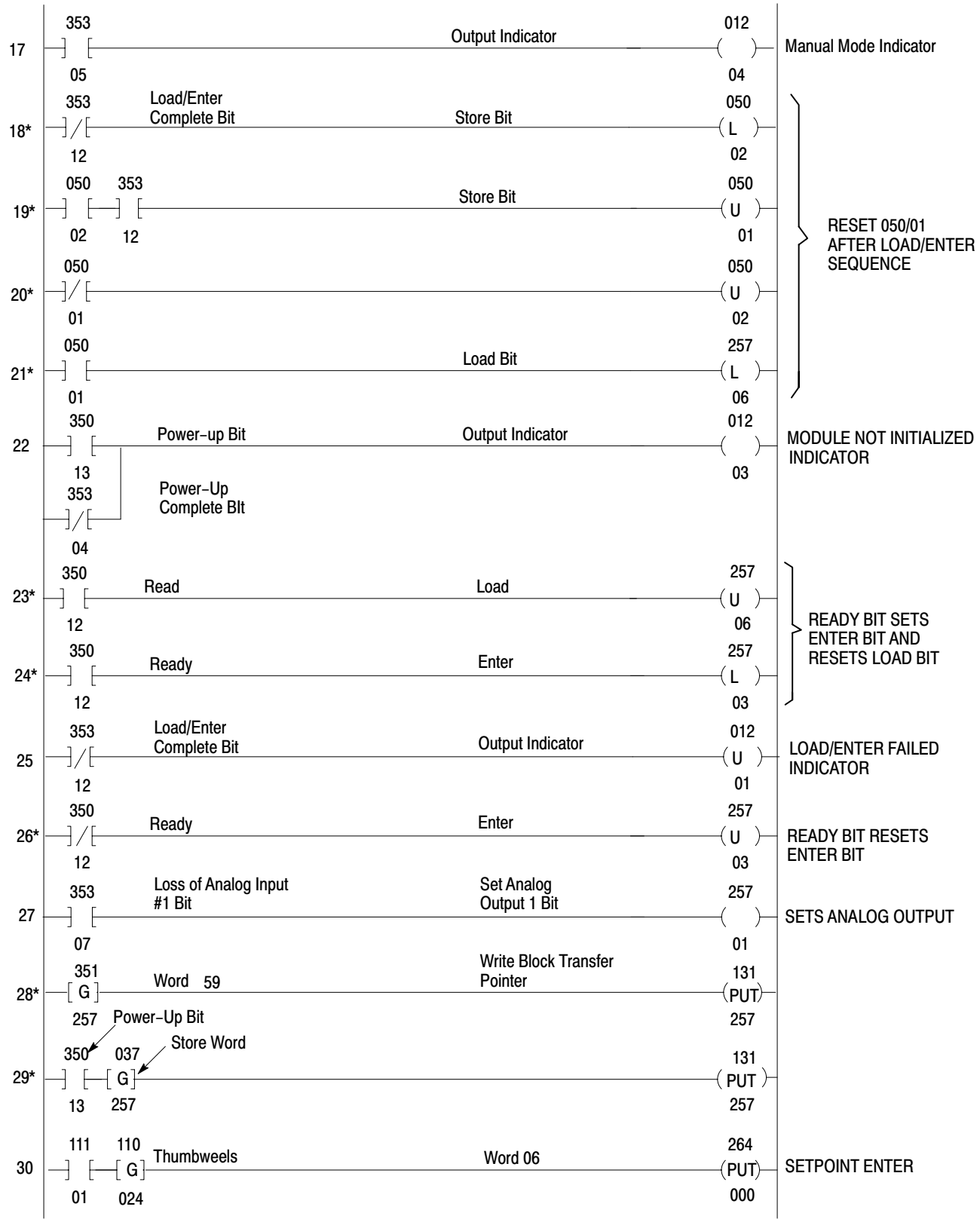
- an alarm condition is detected by the module
- the manual control station is in manual mode
- the PID module is powered and waiting for a load/enter sequence
- the load/enter sequence failed
- a read block transfer is delayed or lost

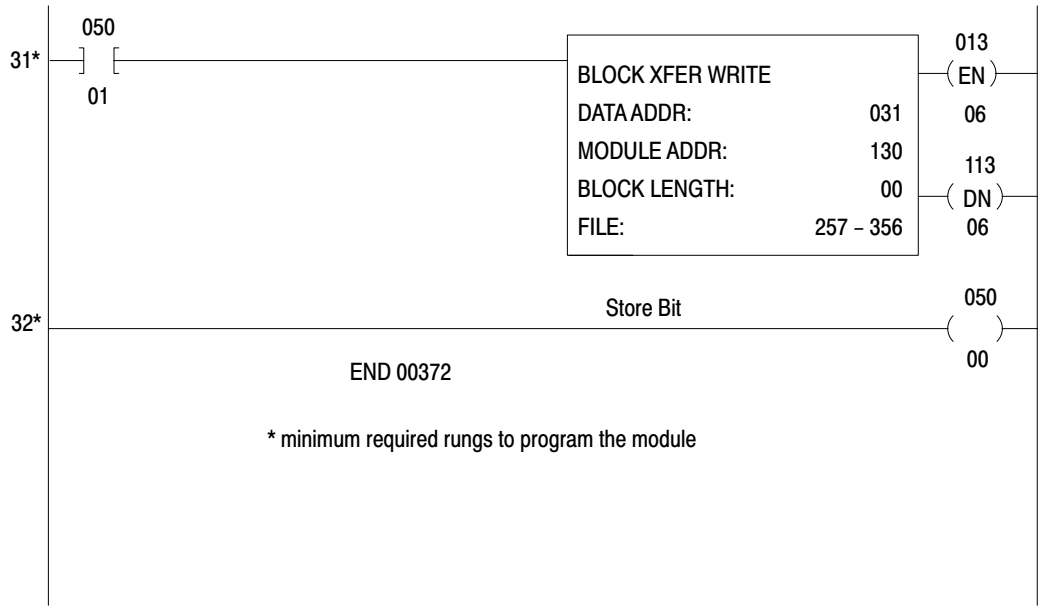
The ladder diagram program for PLC-2 family processors that use block format instructions is presented on the next three pages.

Figure C.2
Ladder Diagram Program, Example 2






17
353 05
Output Indicator
012 04
Manual Mode Indicator
18*
353 12
Load/Enter Complete Bit
Store Bit
050 02
L
19*
050 02
353 12
Store Bit
050 01
U
20*
050 01
050 02
U
21*
050 01
Load Bit
257 06
L
RESET 050/01 AFTER LOAD/ENTER SEQUENCE
22
350 13
Power-up Bit
Output Indicator
012 03
MODULE NOT INITIALIZED INDICATOR
353 04
Power-Up Complete Bit
23*
350 12
Read
Load
257 06
U
24*
350 12
Ready
Enter
257 03
L
READY BIT SETS ENTER BIT AND RESETS LOAD BIT
25
353 12
Load/Enter Complete Bit
Output Indicator
012 01
U
LOAD/ENTER FAILED INDICATOR
26*
350 12
Ready
Enter
257 03
U
READY BIT RESETS ENTER BIT
27
353 07
Loss of Analog Input #1 Bit
Set Analog Output 1 Bit
257 01
SETS ANALOG OUTPUT
28*
351 257
G
Word 59
Write Block Transfer Pointer
131 257
PUT
Power-Up Bit
29*
350 13
037 257
G
Store Word
131 257
PUT
30
111 01
110 024
G
Thumbweels
Word 06
264 000
PUT
SETPOINT ENTER



Program Rung Descriptions

rung 1* — Display rung. It allows the words which control the module's operating characteristics to be displayed or changed using the data monitor mode of the industrial terminal.

rung 2 — When selector switch 111/06 is closed, the soft fault reset bit in the master control word, W01 B10, is set.

rungs 3 thru 5 — When switch 111/00 is closed, storage bit 050/04 is energized for one scan. This bit subsequently is used in rung 8 to initiate a load/enter sequence. The load/enter sequence can be initiated manually at any time.

rung 6* — Annunciator lamp 012/05 will be energized if any one of the first five bits of the status monitor byte is energized, signalling an alarm condition at the module. Bits 05, 06 and 07 are examined to prevent 012/05 from becoming latched during block transfers.

rung 7* When all of the first five bits of the status monitor byte are low signifying no errors, annunciator lamp 012/05 turns off.

rung 8* This rung latches storage bit 050/01 which is used to precondition the read and write block transfer rungs 13 and 31. It can be latched on three separate conditions:

1st Parallel Branch - When 050/04 is energized (refer to the explanation for rungs 3 thru 5, load/enter sequence).

2nd Parallel Branch - When bit 050/00 is low (refer to the explanation for rung 32, power-up load/enter sequence).

3rd Parallel Branch - When bit 012/05 is high (refer to the explanation for rungs 6 and 7, alarm load/enter sequence).

Anytime bit 050/01 is latched, a load/enter sequence is initiated. It is subsequently unlatched upon completion of the sequence (rungs 18 thru 20).

rungs 9 thru 11* Timer 044_8 is a free-running timer which, when timed out, latches storage bit 050/07. This bit is subsequently used in rung 13 as a precondition to the read block transfer instruction. This allows a read block transfer to occur at a time interval determined by the preset value of timer 0448. (This preset value is user-selectable).

Storage bit 050/07 is unlatched by the read block transfer done bit. Note that in rung 9, timer 044_8 is reset during a load/enter sequence because storage bit 050/01 is high.

rung 12* Zeros are loaded into timer/counter address 0328. The boundary tells the PC processor not to look beyond word 0328 for data addresses associated with block transfer instructions.

rung 13* The read block transfer instruction reads the next block of data sent by the PID module and transfers it to the buffer area of the data table, words 233-2568. This rung is executed only when bit 050/01 is high (refer to the explanation for rung 8) or when storage bit 050/07 is high (refer to explanations for rung 9 thru 11).

rung 14* Upon completion of a valid read block transfer (determined by examining the block transfer done bit 113/07), the data from the input buffer is transferred to the status block data table words 347-3708. Identifier bits 16 and 17 of word 2348 are examined for a low logic state to ensure that the input buffer had received valid status data from the PID module.

rung 15 Timer 0438 is the read block transfer watchdog timer. It will begin timing whenever the read block transfer done bit 113/07 is low. Upon completion of a valid read block transfer, the done bit goes high and resets the timer. The preset value of this timer is user-selectable.

rung 16 Annunicator lamp 012/02 illuminated when the read block transfer watchdog timer times out.

rung 17 Annunciator lamp 012/04 illuminates when the manual control station is in manual mode.

rung 18 thru 20* These rungs reset bit 050/01 upon completion of a successful load/enter sequence. Bit 353/12 is the load/enter complete bit. Bit 050/02 is a storage bit which allows 353/12 to toggle from 0 to 1 before resetting050/01.

rung 21* The load bit 257/06 is latched when storage bit 050/01 is high. Bit 050/01 is high. Bit 050/01 is high during a load/enter sequence.

rung 22 The MODULE NOT INITIALIZED indicator 012/03 illuminates when the power-up bit 350/13 is high or the power-up complete bit 353/04 is low.

rung 23* Ready bit 350/12 resets the load bit 257/06.

rung 24* Ready bit 350/12 sets the enter bit 257/03.

rung 25 The LOAD/ENTER FAILED indicator 012/01 will be on when the load/enter complete bit 353/12 is low.

rung 26* This rung resets the enter bit 257/03 when the ready bit 350/12 turns low.

rung 27 Bit 353/07 will go high upon loss of signal at analog input 1. This will energize 257/01 and set the analog output a programmed value in word 2638 module word W05.

rung 28* This rung loads the location of the next data block requested by the module (next block start address) into the block transfer write instruction.

rung 29* If the power-up bit 350/13 is set, the get instruction fetches the dynamic block start address stored in 0378. The put instruction places the dynamic block start address in the block transfer write instruction word 1318(1008 above the data address). This rung will be true only until the first load/enter sequence is executed. When true, it will override rung 28.

rung 30 A 4-digit BCD value residing in data table location 1108 will be loaded into the setpoint word of the dynamic block when pushbutton 111/01 is closed. This rung facilitates user-entry of setpoint values.

NOTE: Although the get/put rung displays only the values of the lower 12 bits in word 1108, it functionally transfers all 16 bits into word 2648/

rung 31* The block transfer write instruction will write data from the file location loaded into word 1318 to the module (the location is determined by rungs 28 and 29). This instruction is executed only when bit 050/01 is high (refer to rung 11).

rung 32* This rung unconditionally energizes storage bit 050/00. It serves to initiate a load/enter sequence on initial power-up of the PC processor, and when PC processor operation is changed from program to run mode. This bit will be low for one program scan at power-up and energized unconditionally thereafter. It is examined in rung 11 for a low logic state and thereby initiates the load/enter sequence.

*minimum required rungs to program the module

Descriptive Figures and Tables

Refer to the following figures and tables which describe the PLC-2 family program.

- data table information showing the storage and instruction address (Table C.A)
- functional bit/word addresses and descriptions (Table C.B)
- data table map showing the dynamic block, loop blocks and status block locations (Figure C.3)
- recommended output annunciators (Table C.C)

Table C.A
Data Table Information

Word Address	Number of Words
Input Buffer Location words $233_{,8}$-256_8	20
Dynamic Block Location words 257_8-277_8	17
Loop 1 Block Location words 300_8-322_8	19
Loop 2 Block Location words 324_8-346_8	19
Status Block Location Word 347_8-370_8	18
Timers/Counter 043_8, 044_8, 143_8 , 144_8	4
Block Transfer Instructions 030_8 , 031_8 , 130_8 , 131_8	4
File-To-File Move Instructions 040_8, 041_8, 140_8. 141_8	4
Storage Words 032_8, 033_8, 037_8, 050_8	4
Total	109
Pushbutton/Selector Switches PB 111/00, PB 111/01, SS 111/04	
OUTPUT INDICATORS 012/01, 012/02, 012/03, 012/04, 012/05	
Storage Bits 050/00, 050/01, 050/02, 050/03, 050/04, 050/07	
Module Location rack 1, module group 3: 113 input image table, 013 output image table	
PC Processor Type PLC-2/30	
Ladder Diagram Program Length 109 words	

Table C.B
Functional Bit/Word Descriptions

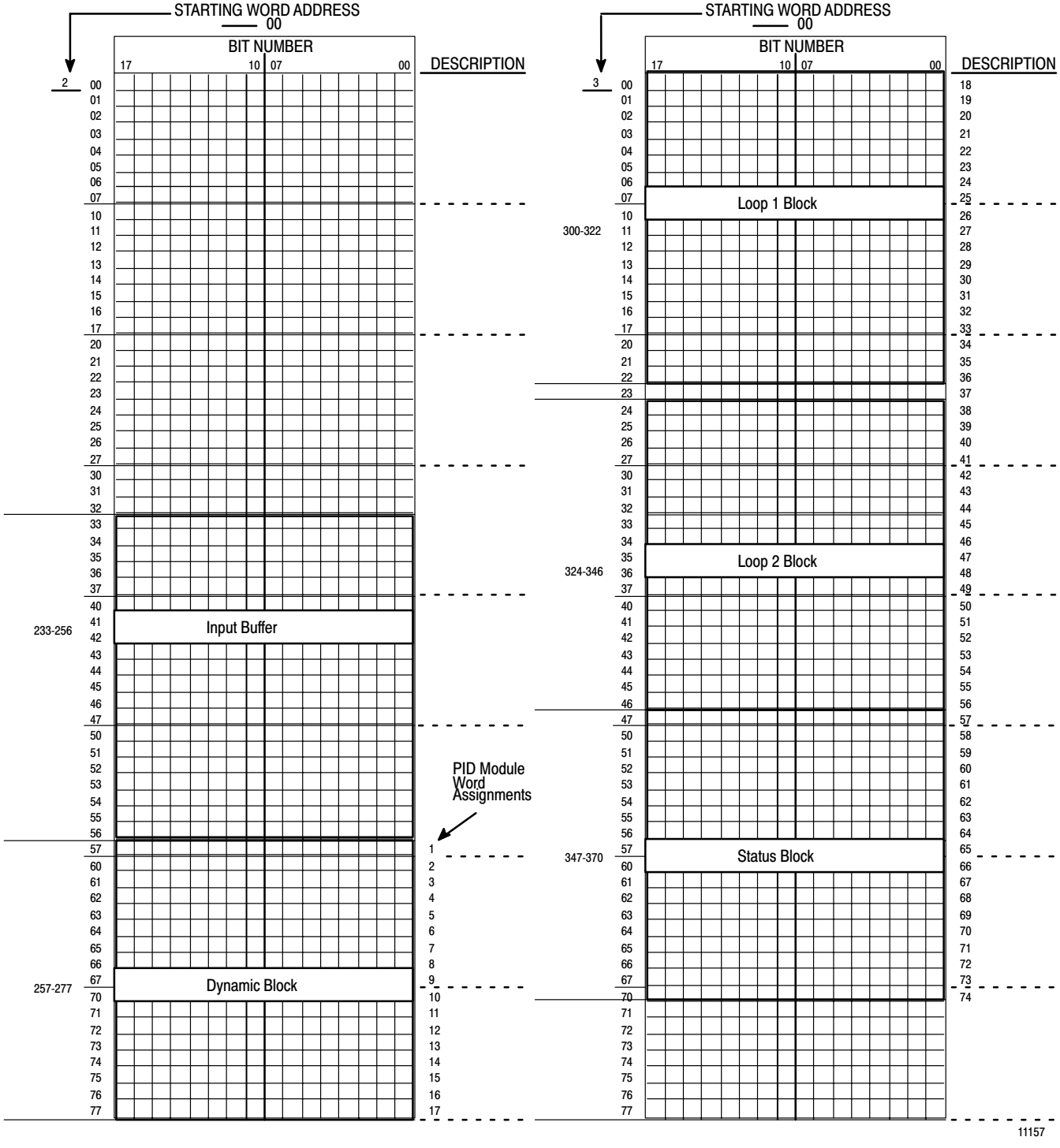
PROGRAM ADDRESS	MODULE ADDRESS [1]		FUNCTION
257/01	W01	B01	When set, allows a programmed value to be downloaded to analog output 1
275/03	W01	B03	Enter bit
257/06	W01	B06	Load bit
350/12	W58	B12	Ready bit
350/13	W58	B13	Power-up bit
353/04	W61	B04	Power-up complete bit
353/05	W61	B05	Set when auto/manual station is in the manual mode
353/07	W61	B07	Set when manual control station is in the manual mode
353/12	W61	B12	Load/enter complete bit
2638	W05		Analog output 1 downloaded from the PC processor
2648	W06		Loop 1 setpoint
3518	W59		Contains data table location of the next data block required by the module

[1] W01 master control word (dynamic block)
W05 word for set analog output 1 (dynamic block)
W06 set point word (dynamic block)
W58 alarm word (status block)
W59 word for next block start address (status block)
W61 status word (status block)

Figure C.3
Data Table Map
Allen-Bradley Programmable Controller
Data Table MAP (128-word)
(Publication 5045 - February, 1982)

PAGE____ OF ____
ADDRESS____ TO ____

PROJECT NAME Example 2 Program
DESIGNER
PROCESSOR PLC-2/30
DATA TABLE SIZE 540



Specific Example

Once the program has been written, specific parameters of the dynamic block and loop block can be entered into the respective data table files. This can be done using the data monitor display mode of the industrial terminal. In ladder diagram (program) mode, place the cursor on the file-to-file move instruction in rung 1 and press the (DISPLAY)(1) keys on the industrial terminal keyboard. The hexadecimal display of the dynamic block and loop blocks will appear on the screen. Enter the selected standard and expanded feature values.

The features and values that have been selected for this example program problem are tabulated below according to the control word in which the features are programmed.

Master Control Word (W01)

Bits 17, 16 = 1	Both identifier bits must be 1.
Bit 15 = 0	Two loops are selected.
Bit 14 = 1	Expanded features are used.
Bit 13 = 0	Calibration bit must be 0.
Bit 12 = 0	Format is BCD.
Bit 11 = 0	Setpoint format is BCD.
Bit 10 = 0	Soft fault is programmed for manual reset. Bit 10 is controlled in rung 2.
Bit 07 = 1	Diagnostics are reported in word W60.
Bit 06	Load bit is controlled by user program.
Bits 05, 04 = 0	Verify bits must be 0.
Bit 03	Enter bit is controlled by user program.
Bit 02 = 0	Set output bit is not used.
Bit 01 = 0	Analog output is set to programmed value if loss of PVinput 1 occurs. Bit 01 is in rung controlled 27.
Bit 00 = 0	Manual request bit is not used.

Loop 1 Control Word A (W18)

Bit 17 = 0	Block identifier must be 0.
Bit 16 = 1	Block identifier must be 1.
Bit 15 = 0	The source of the process variable input is the analog input.
Bit 14 = 0	Square root is not used.
Bit 13 = 0	Error is positive (SP-PV).
Bit 12 = 0	Error limiting is not used.

Bit 11 = 1	Dead band is set to 15 in word W23.
Bit 10 = 1	Integral output is limited to 4000 in wordW26.
Bits 07,06 = 0	Proportional error is not modified.
Bits 05, 04 = 0	Integral error is not modified.
Bit 03 = 0	Derivative error is not modified.
Bit 02 = 0	Derivative output is not limited.
Bit 01 = 0	PID output is not held.
Bit 00 = 0	Bias is not held.

Loop 1 Control Word B W 19

Bit 17 = 0	Bias is added to the output.
Bit 16 = 1	Output is limited to 4050 in word W28 for loop 1.
Bit 15 = 1	Soft fault response is to continue PID control.
Bit 14 = 0	Soft fault response is to continue PID control.
Bit 13 = 0	Soft fault response is to continue PID control.
Bit 12 - 0	Digital filter time x1.
Bits 11,10 = 0	Lead/lag time multiplier is x1.
Bit 07 = 0	Set point sign is positive.
Bits 05,04 = 0	K_P multiplier is x1.
Bits 03,02 = 0	K_I multiplier is x1.
Bits 01,00 = 0	K_D multiplier is x1.

Loop 1 Expanded Control Word W30

Bit 17 = 1	Process variable is scaled.
Bit 16 = 1	Set point is scaled.
Bit 15 = 1	Error is scaled.
Bits 14 thru 00=0	None of these features are used.

Loop 2 Control Word A W38

Bit 17 = 1	Block identifier must be 1.
Bit 16 - 0	Block identifier must be 0.
Bit 15 = 0	Source of the process variable input is the analog input.
Bit 14 = 1	Square root modifies the analog input.
Bit 13 = 0	Error is positive (SP-PV).
Bit 12 = 0	Error limiting is not used.
Bit 11 = 1	Dead band is set to 20 in word W43.

Bit 10 = 0	Integral output limiting is not used.
Bits 07,06 = 1	Proportional error is squared.
Bits 05,04 = 0	Integral error is squared.
Bit 03 = 0	Derivative error is not modified.
Bit 02 = 0	Derivative output is not limited.
Bit 01 = 0	PID output is not held.
Bit 00 = 0	Bias is not held.

Loop 2 Control Word B W39

Bit 17 = 0	Bias is added to the output.
Bit 16 - 0	Output limiting is not used.
Bits 15,14,13=1	If a soft fault occurs, output 2 is set to maximum.
Bit 12 = 0	Digital filter time multiplier is x1.
Bit 11,10=0	Lead/lag time x1.
Bit 7 = 0	Set point sign is positive.
Bit 06 = 0	Setpoint multiplier is x1.
Bits 05 = 1,04=0	Proportional gain multiplier is x10
Bits 03,02=0	Integral gain multiplier is x1.
Bits 01,00=0	Derivative gain multiplier is x1.

Loop 2 Expanded Control Word W50

Bit 17 = 1	Process variable is scaled.
Bit 16 = 1	Set point is scaled.
Bit 15 = 1	Error is scaled.
Bits 14 thru 00=0	None of these features are used.

Selected feature values for this example program have been recorded in worksheets 1,2 and 3. (figures C.4, C.5 and C.6, respectively.) Worksheet 1 represents the dynamic block (data table words 257-277$_8$). The PID module word numbers correspond to the position numbers on the display and are numbered W01 through W17. Worksheet 2 represents the loop 1 block (data table words 300-322$_8$). Worksheet 3 represents the loop 2 block (data table words 324-346$_8$). The PID word numbers (position numbers) are W18 through W36 and W38 through W56, respectively for loop 1 and loop 2. Refer to the data table map (figure C.3) which shows the locations of the consecutive data blocks.

Figure C.4
Worksheet 1 for Dynamic Block

Allen-Bradley Programmable Controller
1771-PD Module Worksheet 1 Dynamic Block

Page 1 of 3

Project Name: Example Program Processor: PLC-2/30
Designer: _____ Data Table Size: 540

DATA TABLE WORD USAGE From 257 to 277

Data Table Word Address	Module Word #	Name	Value	Range	BCD or BIN	Multiplier	Sign
	[3]		17 14 | 13 10 | 07 04 | 03 00				
257	W01	Master Control Word	1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0	FFFF	→	D000 [4]	
260	W02	Control Word		F000	--		
261	W03	Dynamic Block Start Address	0 | 2 | 5 | 07	FFFF	--		
262	W04	Loop 1 Block Start Address	0 | 3 | 0 | 00	FFFF	--		
263	W05	Set Analog Output 1 SET OUT1	2 | 0 | 4 | 28	4095	[1]		
264	W06	Set Point 1 SP1	3 | 0 | 7 | 32	4095/ 9999	[2]	x10 W19 B06 x1	W19 B07- [5] +
265	W07	Proportional Gain 1 K_P1	4 | 5 | 5 | 40	99.99	--	W19 B05.04 x1	[6]
266	W08	Bias 1 BIAS1	0 | 0 | 9 | 06	9999	--		
267	W09	Set Process Variable 1 SET PV1	0 | 0 | 0 | 00	4095	[1]		
270	W10	Set Feedforward Input 1 SET FFI1	0 | 0 | 0 | 00	4095	[1]		
271	W11	Loop 2 Block Start Address	0 | 3 | 2 | 04	FFFF	--		
272	W12	Set Analog Output 2 SET OUT2	1 | 0 | 2 | 14	4095	[1]		

273	W13	Set Point 2 SP2	2 | 5 | 0 | 0	4095/ 9999	[2]	x10 W39 B06 (x1)	W39 B07- [5] (+)
274	W14	Proportional Gain 2 K_P2	0 | 0 | 8 | 5	99.99	--	W39 B05,04 x1	[6]
275	W15	Bias 2 BIAS2	0 | 0 | 2 | 5	9999	--		
276	W16	Set Process Variable 2 SET PV2	0 | 0 | 0 | 0	4095	[1]		
277	W17	Set Feedforward Input 2 SET FFI2	0 | 0 | 0 | 0	4095	[1]		

NOTES:
[1] denotes selection by W 01 B12
[2] denotes selection by W 01 B11
[3] also represents the displayed position number
[4] record Hex value
[5] circle choice
[6] record value

Figure C.5
Worksheet 2 for Loop 1 Block

Allen-Bradley Programmable Controller
1771-PD Module Worksheet 2
Loop 1 Block

Page 2 of 3

Project Name: Example Program Processor: PLC-2/30

Designer: _____ Data Table Size: 540

DATA TABLE WORD USAGE From 300 to 322

Data Table Word Address	Module Word #	Name	Value	Range	BCD or BIN	Multiplier	Sign
	1		17 14 13 10 07 04 03 00				
300	W18	Loop 1 Control Word A	0 1 0 0 0 0 1 1 0 0 0 0 0 0 0 0	FFFF	→	4300 (2)	
301	W19	Loop 1 Control Word B	0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	FFFF	→	6000 (2)	
302	W20	Input Filter Time Constant 1 TA1	0 | 1 | 9 | 0	99.99	--	x10 W19 B12 (x1)	3
303	W21	Maximum Negative Error 1 EMN1	4 | 0 | 9 | 5	4095	--		
304	W22	Maximum Positive Error 1 EMP1	4 | 0 | 9 | 5	4095	--		
305	W23	Dead Band 1 DB1	0 | 0 | 1 | 5	4095	--		
306	W24	Integral Gain 1 K_I1	0 | 6 | 0 | 0	9.999	--	W19 B03,02 x1	4
307	W25	Derivative Gain 1 K_D1	0 | 0 | 0 | 0	99.99	--	W19 B01,00	4
310	W26	Integral Term Limit 1 V_IMAX1	4 | 0 | 0 | 0	9999	--		
311	W27	Derivative Term Limit 1 V_DMAX1	4 | 0 | 9 | 5	9999	--		
312	W28	Minimum Output Limit 1 VMIN1	0 | 0 | 0 | 0	4095	--		

313	W29	Maximum Output Limit 1 VMAX1	4 | 0 | 9 | 5	4095	--		
			17 14 | 13 10 | 07 04 | 03 00				
314	W30	Loop 1 Expanded Control Word	1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	FFFF	→	E000 [2]	
315	W31	Minimum Scaling Value 1 SMIN1	0 | 0 | 5 | 0	9999	--		W30 B04 - (+) [3]
316	W32	Maximum Scaling Value 1 SMAX1	0 | 3 | 0 | 0	9999	--		W30 B03 - (+) [3]
317	W33	Feedforward Offset 1 FFO1	0 | 0 | 0 | 0	9999	--		
320	W34	Feedforward Gain 1 K_F1	0 | 0 | 0 | 0	99.99	--	W30 B07,06	[4]
321	W35	Lead Time Constant 1 TB1	0 | 0 | 0 | 0	99.99	--	W19 B11 x10 / x1	[3]
322	W36	Lag Time Constant 1 TC1	0 | 0 | 0 | 0	99.99	--	W19 B11 x10 / x1	[3]

NOTES:
[1] Also represents the displayed position number
[2] record Hex value
[3] circle choice
[4] recordd value

Figure C.6
Worksheet 3 for Loop 2 Block

Page 3 of 3

Project Name: Example Program Processor: PLC-2/30

Designer: _____ Data Table Size: 540

DATA TABLE WORD USAGE From 324 to 346

Data Table Word Address	Module Word #	Name	Value	Range	BCD or BIN	Multiplier	Sign
	1		17 14 | 13 10 | 07 04 | 03 00				
324	W38	Loop 2 Control Word A	1 0 0 1 | 0 0 1 0 | 1 1 0 0 | 0 0 0 0	FFFF	→	92C0 (2)	
325	W39	Loop 2 Control Word B	0 0 1 1 | 1 0 0 0 | 0 0 0 0 | 0 0 0 0	FFFF	→	3820 (2)	
326	W40	Input Filter Time Constant 2 TA2	0 | 2 | 5 | 0	99.99	--	x10 W39 B12 (x1)	3
327	W41	Maximum Negative Error 2 EMN2	4 | 0 | 9 | 5	4095	--		
330	W42	Maximum Positive Error 2 EMP2	4 | 0 | 9 | 5	4095	--		
331	W43	Dead Band 2 DB2	0 | 0 | 2 | 0	4095	--		
332	W44	Integral Gain 2 K_I2	0 | 1 | 0 | 0	9.999	--	W39 B03,02 x1	4
333	W45	Derivative Gain 2 K_D2	0 | 0 | 0 | 0	99.99	--	W39 B01,00	4
334	W46	Integral Term Limit 2 V_IMAX2	4 | 0 | 0 | 0	9999	--		
335	W47	Derivative Term Limit 2 V_DMAX2	4 | 0 | 9 | 5	9999	--		
336	W48	Minimum Output Limit 2 VMAX2	0 | 0 | 0 | 0	4095	--		
337	W49	Maximum Output Limit 2 VMIN2	4 | 0 | 9 | 5	4095	--		
			17 14 | 13 10 | 07 04 | 03 00				

340	W50	Loop 2 Expanded Control Word	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 [1]	FFFF	→	E000 [2]	
341	W51	Minimum Scaling Value 2 SMIN2	0 | 0 | 0 | 0	9999	--		W50 B04 - (+) [3]
342	W52	Maximum Scaling Value 2 SMAX2	0 | 1 | 5 | 0	9999	--		W50 B03 - (+) [3]
343	W53	Feedforward Offset 2 FFO2	0 | 0 | 0 | 0	9999	--		
344	W54	Feedforward Gain 2 K_F2	0 | 0 | 0 | 0	99.99	--	W50 B07,06	[4]
345	W55	Lead Time Constant 2 TB2	0 | 0 | 0 | 0	99.99	--	W39 B11 x10 x1	[3]
346	W56	Lag Time Constant 2 TC2	0 | 0 | 0 | 0	99.99	--	W39 B10 x10 x1	[3]

NOTES:
[1] also represents the displayed position number
[2] record Hex value
[3] circle choice
[4] record value

Table C.C
Recommended Output Annunciators

DESCRIPTION	FUNCTION
READ BLOCK TRANSFER WATCHDOG Indicator Program Address 012/02	This indicator will illuminate if a read block transfer does not occur within a predetermined time. The time is determined by the preset value selected for the timer instruction 043_8 in rung 15 and is user-selectable. If a read block transfer is not successfully executed withint the preset time, timer 043_8 will time-out and energize indicator 012/02.
LOAD/ENTER FAILURE Indicator Program Address 012/01	This indicator will illuminate in the event of an unsuccessful load/enter sequence. During program execution, this indicator will normally be off. When a load/enter sequence is begun, it will illuminate and will remain on until the sequence is completed (approximately 1 second). If the indicator remains on, then the load/enter sequence failed. (rung 15).
MANUAL MODE Indicator Program Address 012/04	This indicator will illuminiate when the maual control station (if used) is in the manual mode.
STATUS MONITOR BYTE ERROR Indicator Program Address 012/05	This indicator will show that an alarm condition exists at the module. During program execution, this indicator will normally be off. If will illuinate when a condition exists at the module which causes a bit in the status monitor byte to go high. It will remain on until the error condition is corrected. NOTE: When this indicator is on, the program will be executing continuou s load/enter sequences which will allow the source of error be read in the diagnostic & status words. Data must be written to the module to correct the problem. Because the program is executing continuous load/enter sequences, the LOAD/ENTER FAILURE indicator will be flashing on and off. This condition will occur for any error, read and write block transfers can be exectued. However no load/enter sequence will be performed until the soft fault reset bit is set at the module returning the module to the normal operating mode.

Program for PLC-3 Processor

The PLC-3 program for periodic block transfer is presented in Figure 3.7. Worksheets for the Dynamic Block (Figure C.4figure C.4) and Loop Blocks (Figure C.5 and NO TAG) also apply to the PLC-3 program. File storage addresses are listed in Table C.D.

Figure C.7
PLC-3 Periodic Block Transfer Program

RUNG NUMBER RM0

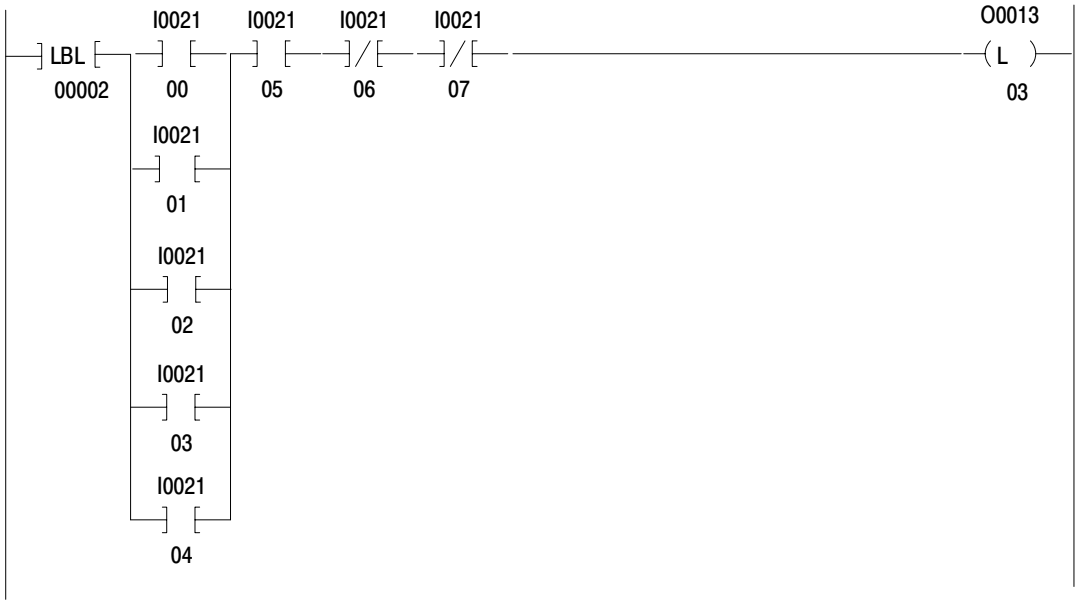
THIS ONE-SHOT TIMER ALLOWS FOR AUTOMATIC EXECUTION OF A LOAD/ENTER SEQUENCE AT PROCESSOR POWER-UP IN ORDER TO INITIALIZE THE 1771-PD MODULE. ONE-SHOT BIT T0000/16 IS ONLY ENERGIZED FOR THE FIRST SCAN OF THE USER PROGRAM AND IS OFF THEREAFTER. IT IS EXAMINED FOR AN 'ON' STATE IN RUNG 4 TO START THE LOAD/ENTER SEQUENCE.

RUNG NUMBER RM1

THIS ONE-SHOT TIMER ALLOWS THE USER TO INITIALIZE A LOAD/ENTER SEQUENCE AT ANY TIME. WHEN THE USER-PROVIDED PUSHBUTTON AT ADDRESS I0012 IS CLOSED, A LOAD/ENTER SEQUENCE IS EXECUTED. ONE-SHOT BIT T0001/16 IS EXAMINED IN RUNG 4 TO START THE SEQUENCE.

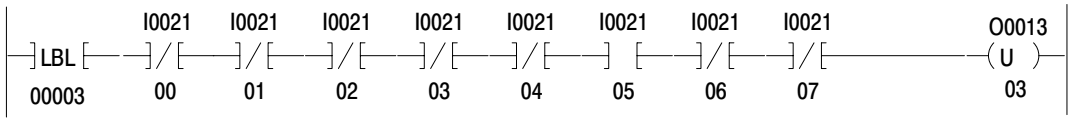
RUNG NUMBER RM2

SHOULD ANY OF THE ALARM-INDICATING BITS (BITS I0021/00 THRU I0021/04) OF THE STATUS MONITOR BYTE BE 'ON', OUTPUT INDICATOR O0013/03 WILL BE LATCHED ON TO INDICATE AN ALARM CONDITION IN THE PROCESS. BIT O0013/03 IS EXAMINED IN RUNG 4 TO INITIATE CONTINUOUS LOAD/ENTER SEQUENCES UNTIL THE ALARM CONDITION IS GONE.



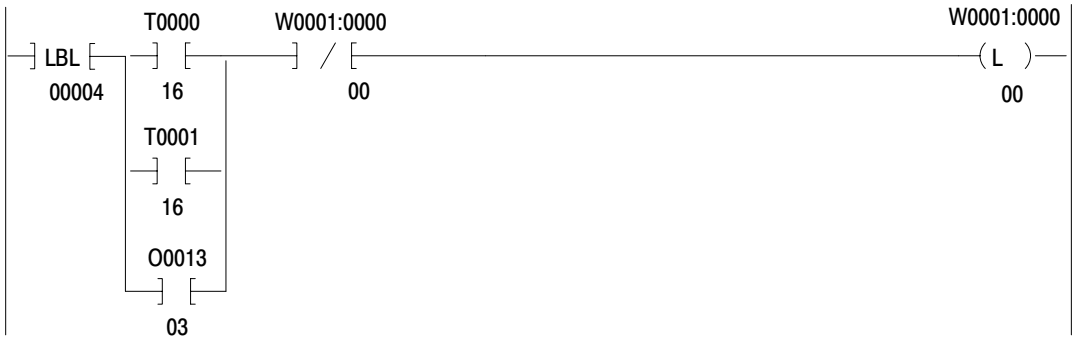
RUNG NUMBER RM3

IF NO ALARM-INDICATING BITS OF THE STATUS MONITOR BYTE ARE ON, THEN OUTPUT ANNUNCIATOR O;13/03 WILL BE OFF.



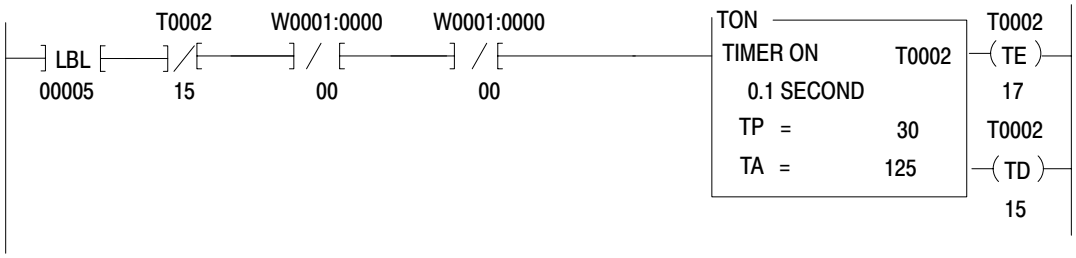
RUNG NUMBER RM4

AN 'ON' STATE OF EITHER OF THE TIMER ONE-SHOT BITS (T0/16 AND T1/16) OR THE STATUS MONITOR BYTE OUTPUT INDICATOR WILL CAUSE STORAGE BIT W0001:0000/00 TO BE LATCHED. THIS BIT IS EXAMINED IN RUNG 15 TO LATCH THE 'LOAD' BIT AND BEGIN THE LOAD/ENTER SEQUENCE.



RUNG NUMBER RM5

THIS FREE–RUNNING TIMER ALLOWS A READ BLOCK TRANSFER TO OCCUR AT A USER SELECTABLE TIME INTERVAL AS DETERMINED BY THE FREE–RUNNING TIMER PRESET VALUE. (*NOTE* – THIS TIMER WILL BE RESET DURING THE EXECUTION OF A LOAD/ENTER SEQUENCE BECAUSE STORAGE BIT W0001:0000 WILL BE ON).



RUNG NUMBER RM 6

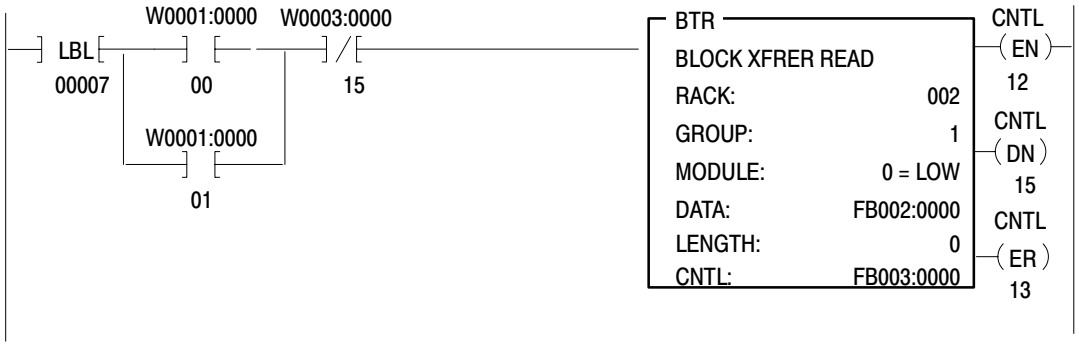
STORAGE BIT W0001:0000/01 IS LATCHED WHEN FREE-RUNNING TIMER T2 'TIMES OUT.' BIT W0001:0000 IS USED AS A PRECONDITION TO THE BLOCK TRANSFER READ INSTRUCTION IN RUNG 7.

Figure C.7 - PLC-3 Periodic Block Transfer Program (Cont.)

Figure C.7 - PLC-3 Periodic Block Transfer Program (Cont.)

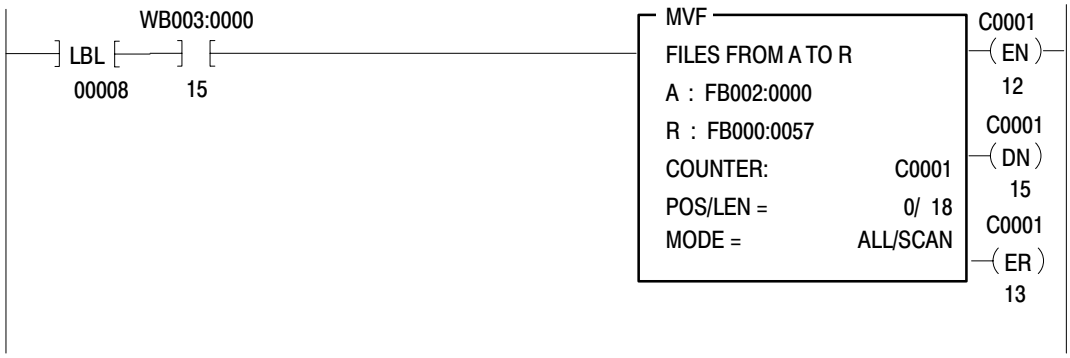
RUNG NUMBER RM7

THIS RUNG READS THE STATUS BLOCK FROM THE 1771–PD MODULE AND TRANSFERS IT INTO A BUFFER FILE (BINARY FILE 2). THIS OCCURS ON A LOAD/ENTER REQUEST (STORAGE BIT W0001:0000/00 SET) OR A TIMER INITIATED REQUEST (BIT W0001:0000/01 SET). (*NOTE* - BLOCK TRANSFER RUNG MUST BE CONDITIONED WITH AN 'XIO' OF ITS RESPECTIVE 'DONE' BIT.).



RUNG NUMBER RM8

UPON COMPLETION OF A VALID 'READ' OF THE STATUS BLOCK INTO THE BUFFER AREA (SIGNIFIED BY AN 'ON' CONDITION OF THE READ BLOCK TRANSFER 'DONE' BIT), THE STATUS BLOCK IS MOVED FROM THE FBUFFER AREA TO THE USER–SPECIFIED STATUS AREA.



RUNG NUMBER RM9

STORAGE BIT W0001:0000/01 IS UNLATCHED BY THE READ BLOCK TRANSFER 'DONE' BIT.

RUNG NUMBER RM10

SHOULD A SUCCESSFUL READ BLOCK TRANSFER NOT OCCUR WITHIN THE USER–SPECIFIED PRESET TIME, READ BLOCK TRANSFER 'WATCHDOG' TIMER WILL 'TIME-OUT' TO INDICATE A READ BLOCK TRANSFER FAILURE. (*NOTE* – RUNG IS CONDITIONED BY AN 'XIO' OF THE READ BLOCK TRANSFER 'DONE' BIT).

RUNG NUMBER RM11

OUTPUT ANNUNCIATOR O0013/00 WILL ENERGIZE TO INDICATE A READ BLOCK TRANSFER FAILURE WHEN TIMER T3 TIMES OUT.

RUNG NUMBER RM12

WHEN THE 'LOAD/ENTER COMPLETE' BIT (B:61/12) IS OFF (THIS OCCURS ONLY DURING THE EXECUTION OF A LAOD ENTER SEQUENCE), LATCH STORAGE BIT W0001:0000

RUNG NUMBER RM13

WHEN STORAGE BIT W0001:000/02 IS LATCHED (SEE RUNG 12) AND 'LOAD/ENTER COMPLETE' BIT IS SET IMMEDIATELY AFTER EXECUTION OF LOAD/ENTER SEQUENCE) THEN UNLATCH STORAGE BIT W0001:0000/00. (SEE RUNG 4).

RUNG NUMBER RM14

WHEN STORAGE BIT W0001:0000/00 IS UNLATCHED, RESET STORAGE BIT W0001:0000/02, (SEE RUNG 12).

RUNG NUMBER RM15

WHEN STORAGE BIT W0001:0000/00 IS LATCHED (SEE RUNG 4), LATCH THE 'LOAD' BIT TO START THE LOAD/ENTER SEQUENCE.

RUNG NUMBER RM16

OUTPUT ANNUNCIATOR O0013/01 WILL ENERGIZE TO INDICATE THAT THE 1771-PD MODULE IS NOT INITIALIZED. THE RUNG IS CONDITOINED BY THE 'POWER–UP' BIT AND THE 'POWER–UP COMPLETE' BIT.

RUNG NUMBER RM17

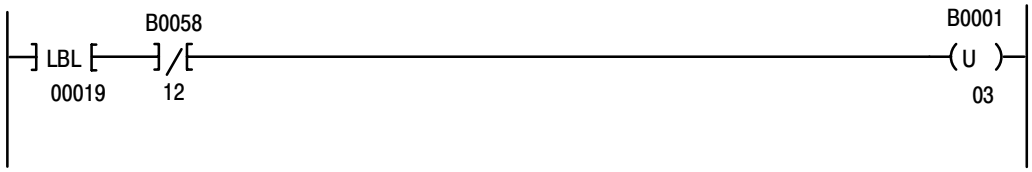
DURING A LOAD/ENTER SEQUENCE, THE 'READY' BIT WILL SET THE 'ENTER BIT AND RESET THE 'LOAD' BIT.

RUNG NUMBER RM18

OUTPUT ANNUNCIATOR O0013/02 WILL ENERGIZE BRIEFLY DURING THE EXECUTION OF A MNAULLY INITIATED LOAD/ENTER SEQUENCE (SEE RUNG 1). IT WILL ALSO FLASH REPEATEDLY IF THE STATUS MONITOR BYTE INDICATES AN ALARM CONDITION (SEE RUNG 2). IN EITHER CASE, SHOULD IT REMAIN ENERGIZED (NOT FLASHING), THEN THE LOAD/ENTER SEQUENCE FAILED. THE RUNG IS CONDITIONED BY THE 'LOAD/ENTER COMPLETE' BIT..

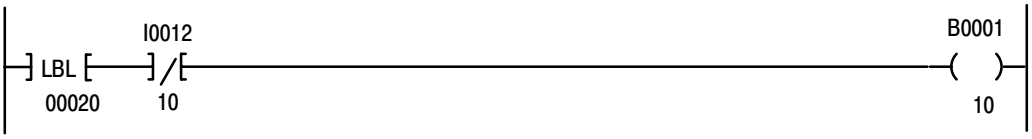
RUNG NUMBER RM19

UPON SUCCESSFUL COMPLETION OF THE LOAD/ENTER SEQUENCE, THE 'READY' BIT RESETS THE 'ENTER' BIT..



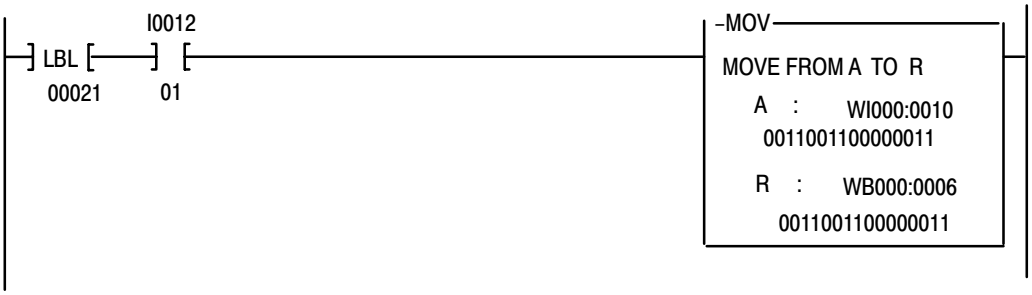
RUNG NUMBER RM20

THIS RUNG GIVES THE USER MANUAL CONTROL OVER THE 'SOFT FAULT RESET' BIT VIA SELECTOR SWITCH I0012/10.



RUNG NUMBER RM21

VALUES FROM THUMBWHEELS (REGISTER 'A') ARE MOVED INTO THE SETPOINT WORD (B000:0006) PUSHBUTTON I0012/01 IS CLOSED.



RUNG NUMBER RM22

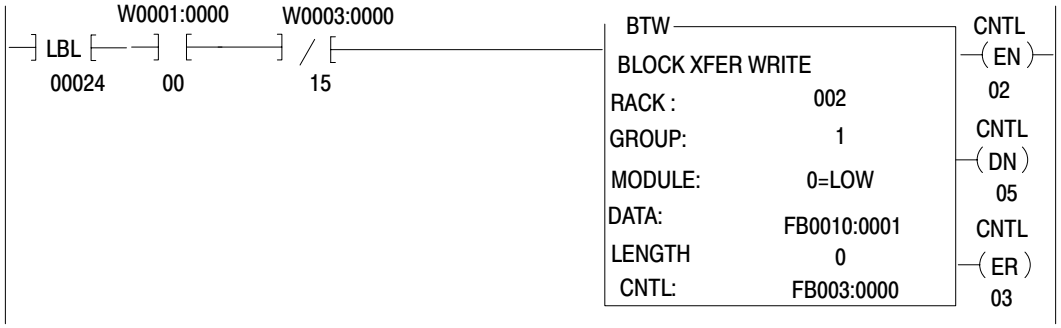
THIS RUNG MOVES THE STARTING DATA TABLE ADDRESS OF THE NEXT BLOCK OF PARAMETERS REQUESTED BY THE 1771–PD MODULE INTO THE 4TH WORD OF THE BLOCK TRANSFER CONTROL FILE. THIS ALLOWS THE BLOCK TRANSFER WRITE INSTRUCTION TO SEND THE CORRECT FILE TO THE MODULE.

RUNG NUMBER RM23

AT POWER–UP, THE STARTING DATA TABLE ADDRESS OF THE DYNAMIC BLOCK STORED IN B000:0000 (REGISTER 'A') IS MOVED INTO THE 4TH WORD OF THE BLOCK TRANSFER CONTROL FILE. CONDITIONED BY THE 'POWER–UP' BIT (B0058/13), THIS RUNG IS EXECUTED ONLY WHILE THE MODULE IS IN THE POWER–UP MODE AND IS OVERRIDDEN BY THE RM22 THEREAFTER.

RUNG NUMBER RM24

THIS RUNG WRITES EITHER THE DYNAMIC OR THE LOOP BLOCKS TO THE 1771-PD MODULE AS DICTATED BY RUNGS 22 AND 23. CONDITIONED BY STORAGE BIT W0001:0000/00, IT IS EXECUTED ONLY DURING A LOAD/ENTER SEQUENCE. (*NOTE* - BLOCK TRANSFER RUNGS MUST BE CONDITIONED BY AN 'XIO' OF THEIR RESPECTIVE 'DONE' BITS).



RUNG NUMBER RM25

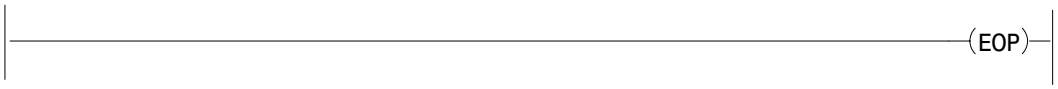


Table C.D
PLC-3 File Storage Addresses
(shown in hex)

Start = WB000:0000

Word number	0	1	2	3	4	5	6	7
00000	**0001**	**E180**	0000	**0001**	**0012**	0000	**3303**	**0050**
00008	0000	0000	0000	**0026**	0000	0000	0000	0000
000116	0000	0000	**4000**	0000	0000	0000	**4095**	0000
00024	0000	0000	0000	0000	0000	**4095**	0000	0000
00032	0000	0000	0000	0000	0000	0000	**8000**	0000
00040	0000	0000	0000	0000	0000	0000	0000	0000
00048	0000	0000	0000	0000	0000	0000	0000	0000
00056	0000	0000	0000	**0001**	0000	**0450**	**2203**	**1101**
00064	**1100**	**1100**	0000	0000	0000	0000	0000	0000
00072	0000	0000	0000	0000	0000	0000	0000	0000

Dynamic Block - binary file 0, words 1 thru 17

start location: 00000000 00000001 in binary, 0001 in hex

Loop 1 Block - binary file 0, words 18 thru 36

start location: 00000000 00010010 in binary, 0012 in hex

Loop 2 Block - binary file 0, words 38 thru 56

start location: 00000000 00100110 in binary, 0026 in hex

Status Block - binary file 0, word 57 thru 74

Input Buffer - binary file 2, words 0 thru 20

Block Transfer Control File - Binary file 3

Module Location: rack 2, module group 1

NOTE: Block transfer control file must be the same for the read and write block transfer instructions.

Binary file 0 word 0 is used to store the dynamic block start address (rung I3 in the continuous block transfer program, rung 23 in the periodic block transfer program).

Appendix D

Summary Word and Bit Tables

Summary Word and Bit Tables

The following tables provide summary references to the word and bit definitions found in chapter 3.

Word/Bit Reference

Summary of Value Words

Master Control Word W01

Control Word A W18 (W38)

Control Word B W19 (W39)

Expanded Control Word W30 (W50)

Alarm Word W58

Status Monitor Byte

Loop Status Word W61 (W68)

Table D.A
Word/Bit Reference

Word or Bit Title	Word Abbr.	Word	Bit	Pg
Alarm bit		SMB	B04	3–50
Alarm conditions, see limit conditions				3–52
Alarm word		W58		3–28
Analog input	READ IN	W64(W71)		3–28
Bias	BIAS	W08(W15)		3–12,3–13
sign bit*		W30(W50)	B01	3–26
source bit*		W30(W50)	B02	3–26
V_{PID} +/x bias bit		W19(W39)	B17	3–18
Block identifier bits				
control word A, Loop 1		W18	B17=0 B16=1	3–15
control word A, Loop 2		W38	B17=1 B16=0	3–15
master control word		W01	B17=B16=1	3–8
status word		W58	B17=B16=0	3–28
Block start address				
dynamic block		W03		3–11
loop block		W04(W11)		3–11,3–13
read next block		W59		3–30
Calibration				
enable bit		W01	B13	3–8
input select bits		W02	B17,B16	5–7
Cascade bit*		W30	B00	3–26
Control word		W02		3–11
Control Word A		W18(W38)		3–15
Control Word B		W19(W39)		3–18
Dead band	DB	W23(W43)		3–22
control bit		W18(W38)	B11	3–17
Decouple bit*		W30	B14	3–25
Derivative term	V_D			
error source bit		W18(W38(	B03	3–17
gain	K_D	W25(W45)		3–22
limit	V_DMAX	W27(W47)		3–23
limit bit		W18(W38)	B02	3–18
multiplier bits		W18(W39)	B01,B00	3–21
Enter bit		W01	B03	3–11
Expanded control word		W30(W50)		3–23

Word or Bit Title	Word Abbr.	Word	Bit	Pg
Expanded feature bit				
see standard/				
expanded features bit		W01	B14	3–8
Feedforward				
gain*	K_F	W34(W54)		3–26
input set value	SET FFI	W10(W17)		3–12,3–14
offset*	FFO	W33(W53)		3–26
Value	READ FFV	W67(W74)		3–38
Feedforward bits				
gain multiplier*		W30(W50)	B07,B06	3–25
input sign*		W30(W50)	B12	3–25
input source*		W30(W50)	B13	3–25
input square root*		W30(W50)	B11	3–25
sign		W61(W68)	B13	3–25
term multiplier*		W30(50)	B10	3–25
Format bits				
BCD/binary,analog				
terms except SP		W01	B12	3–10
BCD/binary, SP		W01	B11	3–10
Gain				
derivative	K_D	W25(W45)		3–22
feedforward	K_F	W34(W54)		3–26
integral	K_I	W24(W44)		3–22
proportional	K_P	W07(W14)		3–12,3–13
Gain multiplier bits				
derivative		W19(W39)	B01,B00	3–21
feedforward		W30(W50)	B07,B06	3–25
integral		W19(W39)	B03,B02	3–21
proportional		W19(W39)	B05,B04	3–21
Hold bits				
bias		W18(W38)	B00	3–18
PID calculation		W18(W38)	B01	3–18
Integral term	V_I			
error select bits		W18(W38	B05,B04	3–17
gain	K_I	W24(W44)		3–22
limit	V_IMAX	W26(W46)		3–22
limit bit		W18(W38)	B10	3–17

Word or Bit Title	Word Abbr.	Word	Bit	Pg
multiplier bits		W19(W39)	B03,B02	3–21
Lead/lag bit*		W30(W50)	B05	3–25
Limit bits				
derivative term		W18(W38)	B02	3–18
error max/min		W18(W38)	B12	3–17
integral term		W18(W38)	B10	3–17
output max/min		W19(W39)	B16	3–18
Limit condition bits				
E<DB		W61(W68)	B11	3–25
E<EMN		W61(W68)	B15	3–25
E>EMP		W61(W68)	B14	3–25
V>VMAX		W61(W68)	B00	3–37
V<VMIN		W61(W68)	B01	3–37
V_DD>VDMAX		W61(W68)	B02	3–37
V_I>VIMAX		W61(W68)	B10	3–35
V_P>4095		W61(W68)	B03	3–37
Limit values				
derivative term	V_DMAX	W27(W47)		3–23
error(+)max	EMP	W22(W42)		3–21
error(–)max	EMP	W21(W41)		3–21
integral term	V_IMAX	W26(W46)		3–22
output max	VMAX	W29(W49)		3–23
output min	VMIN	W28(W48)		3–23
scaling max*	SMAX	W32(W52)		3–26
scaling min*	SMIN	W31(W51)		3–26
Load bit		W01	B06	3–10
Load/enter complete bit		W61	B12	3–25
Loop error	ERROR	W62(W69)		3–37
polarity				
(direct/reverse)bit		W18(W38)	B13	3–15
scaling bit*		W30(W50)	B15	3–25
sign bit		W61(W68)	B17	3–35
Local error limits				
limit enable bit		W18(W38)	B12	3–17
max negative limit	EMN	W21(W41)		3–21
max positive limit	EMP	W22(W42)		3–21
Loop features bit		W01	B14	3–8

Word or Bit Title	Word Abbr.	Word	Bit	Pg
Loop select bit 1 or 2				
loops		W01	B15	3–8
Looptime/diagnostic bit		W01	B07	3–10
Looptime/diagnostic				
word		W60		3–30
Loss of input bit				
analog		W61(W68)	B07	3–35
tieback		W61(W68)	B06	3–36
either one		SMB	B02	3–51
+15V DC		W58	B11 and	3–30
		SMB	B01	3–51
Manual mode bit		W61(W68)	B05	3–37
Manual request bit		W01	B00	3–11
Output	V			
read loop	READ V	W63(W70)		3–37
set value	SET OUT	W05(W12)		3–11,3–13
set output bit		W01	B01(B02)	3–11
Output limits				
limit enable bit		W19(W39)	B16	3–18
max limit	VMAX	W29(W49)		3–23
min limit	VMIN	W28(W48)		3–23
Power–up				
power–up bit		W58	B13 and	3–28
		SMB	B03	3–51
power–up complete bit		W61	B04	3–37
Process variable	PV	W65(W72)		3–38
set value	SET PV	W09(W16)		3–12,3–13
sign of scaled PV bit		W61(W68)	B16	3–35
scaling bit*		W30(W50)	B17	3–23
source bit		W18(W38)	B15	3–15
square root bit		W18(W38)	B14	3–15
Programming error bits				
dynamic block		W58	B15	3–28
loop block		W58	B14	3–28
Programming Error				
codes		W01	B07=1	3–10
upper byte		W60		3–32

Word or Bit Title	Word Abbr.	Word	Bit	Pg
lower byte		W60		3–32
Proportional term	V_P			
gain	K_P	W07(W14)		3–12,3–13
gain multiplier bits		W19(W39)	B05,B04	3–21
error select bits		W18(W38)	B07,B06	3–17
Ready bit		W58	B12	3–28
Scaling*				
max value	SMAX	W32(W52)		3–26
min value	SMIN	W31(W51)		3–26
error scaling bit		W30(W50)	B15	3–25
PV scaling bit		W30(W50)	B17	3–23
SP scaling bit		W30(W50)	B16	3–23
x10 multiplier bit		W19(W39)	B06	3–20
sign bit max scale		W30(W50)	B03	3–26
sign bit min scale		W30(W50)	B04	3–25
Set point	SP	W06(W13)		3–12,3–13
scaling bit*		W30(W50)	B16	3–23
scaled sign bit*		W19(W39)	B07	3–20
Soft fault bit		W58	B10 and	3–10
		SMB	B00	3–51
mode select bits		W19(W39)	B15,B14,B13	3–18
reset bit		W01	B10	3–10
Status word		W61(W68)		3–30
Status monitor byte		SMB		3–50
Tieback input	READ TIE	W66(W73)		3–38
Time constant				
input filter	TA	W20(W40)		3–21
lag filter*	TC	W36(W56)		3–27
lead filter*	TB	W35(W55)		3–26
TA multiplier bit		W19(W39)	B12	3–20
TB multiplier bit*		W19(W39)	B11	3–20
TC multiplier bit*		W19(W39)	B10	3–20
Verify code		W01	B05=B04=0	3–11
*The expanded features bit W01 B14 must be set = 1 in order to use these features.				

Table D.B
Summary of Value Words

Word	Abbr	Format	Range	Multiplier Bit W19(W39)	Sign Bit W19 (W39)	Scaling Bit W30 (W50)	Enable Bit
Dynamic Block							
W05(W12)	SET OUT	W01 B12	0–4095			W01 B01(B02)	
W06(W13)	SP	W01 B11	0–4095				
	scaled [1]	BCD	± 9990	B06	B07, B16		
W07(W14)	K_P	BCD	0–9999	B05, B04			
W08(W15)	BIAS	BCD	± 9999		B01		W30(W50) B02
W09(W16)	SET PV	W01 B12	0–4095				W18(W38) B15
W10(W17)	SET FFI [1]	W01 B12	4095		B12		W30(W50) B13
Loop Blocks							
W20(W40)	TA	BCD	0–999.9	B12			
W21(W41)	EMN	BCD	0–4095				W18 (W38)B12
W22(W42)	EMP	BCD	0–4095				W18(W38)B12
W23(W43)	DB	BCD	0–4095				W18(W38)B11
W24(W44	K_I	BCD	0–999.9	B03, B02			
W25(W45)	K_D	BCD	0–9999	B01, B00			
W26(W46)	V MAX	BCD	0–9999			W18(W38)B10 [2]	
W27(W47)	V MAX	BCD	0–9999				W18(W38)B02
W28(W48)	VMIN	BCD	0–4095				W19(W39)B16
W29(W49)	VMAX	BCD	0–4095				W19(W39)B16
W31(W51)	SMIN [1]	BCD	± 99990	B06	B04	B17, B16, B15	
W32(W52)	SMAX [1]	BCD	±99990	B06	B03	B17, B16, B15	
W33(W53)	FFO [1]	BCD	0–9999				
W34(W54)	K_F [1]	BCD	0–9999	W30(W50) [2]			
				B07, B06			
W35(W55)	TB [1]	BCD	0–999.9	B11			W30(W50)B05
W36(W56)	TC [1]	BCD	0–999.9	B10			W30(W50)B05
Status Block							
W62(W69)	ERROR	BCD	± 4095				
	scaled [1]	BCD	± 99990	B06	W61 (W68) B17 B15 [2]		
W63(W70)	READ V	W01 B12	0–4095				
W64(W71)	READ IN	W01 B12	0–4095				
W65(W72)	READ PV	BCD	0–4095				
	scaled [1]	BCD	± 9999	B06	W61 (W68) B16 B17 [2]		
W66(W73)	READ TIE	W01 B12	0–4095				

W67(W74)	READ FFV	BCD	±9999		W61 (W68) B13 [2]	
[1] The expanded features bir W01 B14 musr be set to use these features.						
[2] Word and bit numbers such a W30(W50)B07,B06 are independent of the word nubmer at the top of the column.						

Table D.C
Master Control Word W01

Bit	Title	Status
B17,B16	Block identifier	0=not allowed
B15	Loop select	0=both loops
		1=loop 1, only
B14	Standard/expanded features	0=standard
		1=expanded
B13	Calibration	0=normal operation
		1=calibration
B12	Binary/BCD format	0=BCD W05,W09,W10,W12,W16,W17
		1=Binary W63,W64,W66,W70,W71,W73
B11	Set point format	0=BCD W06(W13)
		1=binary
B10	Soft fault reset	0=reset
		1=enable
B07	Loop time/diagnostic	0=loop time
		1=diagnostic W60
B06	Load	0=reset 1=enable
B05,B04	Verify	0=normal operation
		1=undefined
B03	Enter	0=reset
		1=enable
B02	SET OUT2	0=reset
		1=enable SET OUT2 in W12
B01	SET OUT1	0=reset
		1=enable SET OUT1 in W05
B00	Set manual request	0=reset
		1=enables contact output

Table D.D
Control Word A W18(W38)

Bit	Title	Status
B17	Block identifier	0 in W18
		1 in W38
B16	Block identifier	0 in W38
		1 in W18
B15	Source of PV	0=analog hardware input
		1=PC processor, W09(W16)
B14	Square root of PV	0=reset
		1=enable
B13	Error polarity	0=SP–PV direct acting
		1=PV–SP reverse acting
B12	Error limit	0=rest
		1=enable EMN in W21(W41) and EMP in W22(W42)
B11	Dead band	0=reset
		1=enable DB in W23(W43)
B10	Maximum integral term limit	0=reset
		1=enables VIMAX in W26(W46)
B07,B06	Proportional term error	00=E
		01=2/3E + 1/3E@
B05,B04	Integral term error	10=1/3E + 2/3E@
		11=E@
B03	Derivative term error	0=error
		1=PV
B02	Maximum derivative term limit	0=reset
		1=enables VDMAX in word W27(W47)
B01	Hold PID calculation	0=reset
		1=hold VPID last value
B00	Hold bias	0=reset
		1=hold BIAS last value

Table D.E
Control Word B W19(W39)

Bit	Title	Status
B17	VPID+/xBias	0=for V=VPID + BIAS
		1= for V (VPID X BIAS)/4095
B16	Output Limiting	0=reset
		1= Limits output V to V MIN in W28(W48) and to V MAX in W29(W49)
B15,B14,		
B13	Soft fault mode selection	000=Output goes to minimum value (+1V DC or +4mA).
		001=Output holds last state.
		010=Output goes to SET OUT value in W05(W12) if W01
		B01(B02) = 1. If = 0, PID control continues.
		100=PID control continues or it resumed if output had been set.
		111= Output goes to maximum value (5V DC or +20mA).
B12	TA multiplier	0=x1
		1=x10 Input time constant TA is stored in W20(W40).
B11	TB multiplier	0=x1
		1=x10 Lead time constant TB is stored in W35(W56).
B10	TC multiplier	0=x1
		1=x10 Lag time constant TC is stored in W36(W56).
B07	Scaled SP sign	0=+
		1=– Set point is stored in W06(W13).
B06	Scaling word multiplier	0=x1
		1=x10 for W06(W13, W31(W51, W32(W52, W62(W69) and
		W65(W72) when scaled
B05,B04	Proportional gain	
	multiplier for W07	
	(W14)	00=x1
		01=divided by 10
B03,B02	Integral gain multiplier for W24(W44)	10=x10 Multiplier codes 00 thru 11 apply to bits B05 thru B00. 11=x100
B01,B00	Derivative gain multiplier for W25(W45)	

Table D.F
Expanded Control Word W30(W50)

Bit	Title	Status
B17	PV scaling	0=reset
		1=PV in W65(W72) is scaled.
B16	SP scaling	0=reset
		1=SP in W06(W13 is scaled.
B15	Error scaling	0=reset
		1=ERROR in W62(W69) is scaled.
B14	Decouple	0=reset
		1=Loop 1 VPID overrides loop 2 FFI. Used for W30, only. W50 B14 =0
B13	Source of FFI	0=SET FFI in W10(W17)
		1=tieback hardware input
B12	FFI sign	0=Feedforward input in positive.
		1=negative sign
B11	FFI square root	0=reset 1=normalized square root
B10	Feedforward term multiplica-tion	0=reset 1=KFx(FFI +FFO), KF is in W34(W54).
B07,B06	Feedforward gainmultiplier	See code for W19(W39)B05 thru B00.
B05	Lead/lag	0=reset
		1=TB in W35(W55)and TC in W36(W56) are enabled.
B04	Minimum scaling sign	0=SMIN in W31(W51) is positive.
		1=negative sign
B03	Maximum scaling sign	0=SMAX in W32(W52) is positive. 1=negative sign.
B02	Source of Bias	0=feedforward term FFV
		1= PC processor, W08(W15)
B01	Bias (FFV) sign	0=Bias (FFV) sign is not changed
		1=reverse sign
B00	Cascade	0=reset
		1=Cascades the output of loop 1 into the set point of loop 2 W50 B00 =0.

Table D.G
Alarm Word W58

Bits	Title	Status
B17,B16	Block identifier	will be 0
B15	Dynamic block error	0=no error
		1=programming error
B14	Loop block error	0=no error
		1=programming error
B13	Power–up	0=Dynamic block is received.
		1=Memory is clear, ready for LE sequence.
B12	Ready	0=normal
		1=Load portion of LE sequence is complete, ready for enter portion.
B11	Loss of +15V DC	0=normal
		1=loss of +15V DC
B10	Soft fault mode	0=normal mode
		1=soft fault mode
B07 thru		
B00	Future use	will be 0

Table D.H
Status Monitor Byte

Bit No.	Title	Status
B07,B06	Precondition	0=Byte is valid.
		1=invalid byte
B05	Precondition	0=Byte is invalid
		1=valid byte
B04	Alarm	0=no alarm condition
		1=An alarm condition is reported in loop status word W61(W68).
B03	Power–up	0=Dynamic block is received.
		1=Memory is clear, ready for LE sequence. (SMB B03 mirrors the status of W58
B13).		
B02	Loss of input	0=Signal is present
		1=loss of analog input or tieback input (under most circumstances)
B01	Loss of +15V DC	0=normal
		1=loss of +15V DC (SMB B01 mirrors the status of W58 B11).
B00	Soft fault mode	0=normal mode
		1=soft fault mode (SMB B00 mirrors the status of W58 B10).

Table D.I
Loop Status Word W61(W68)

Bit. No.	Title	Status
B17	Sign of loop error	0=ERROR in W62(W69) is positive.
		1=negative sign
B16	Sign of scaled PV	0=PV in W65(W72) is positive.
		1=negative sign
B15	ERROR<EMN	0=normal for ERROR in W62(W69)
		1=undershoots EMN in W21(W41)
B14	ERROR>EMP	0=normal for ERROR in W62(W69)
		1=exceeds EMP in W22(W42)
B13	Sign of FFV	0=FFV in W67(W74) is positive.
		1=negative sign
B12	Load/enter complete	0=reset by dynamic block transfer
		1=LE sequence completed
B11	ERROR within dead band	0=ERROR is W62(W69) exceeds DB
		1=ERROR is within DB W23(W43)
B10	VI\VIMAX	0=normal for ERROR in W62(W69)
		1=VI exceeds VIMAX in W26(W46)
B07	Loss of analog input	0=input present in W64(W71)
		1=input lost
B06	Loss of tieback input	0=input present in W66(W73)
		1=input lost
B05	Manual mode	0=PID control
		1=manual mode
B04	Power-up complete	0=reset at start of LE power-up
		1=power-up LE sequence completed
B03	VP\4095	0=normal for VP
		1=VP exceeds 4095.
B02	VD VDMAX	O=normal for VD
		1=VD exceeds VDMAX in W27(W47).
B01	V \ VMIN	0=normal for V
		1=V undershoots VMIN in W28(W48).
B00	V \ VMAX	0=normal for V
		1=V exceeds VMAX in W29(W49).

Appendix E

Comparing ISA 1771-PD Algorithms

The ISA standard algorithm and the Allen-Bradley 1771-PD algorithm are different although they achieve the same closed loop control. By understanding the differences, you can convert proportional gain, reset and rate values from ISA standard to equivalent 1771-PD gain values.

ISA Standard Algorithm

The equation for PID closed loop control is:

$$V_O = K_C(E) + K_C/T_I/(E)dt + K_C(T_D)d(E)/dt$$

Where K_C = controller gain
$1/T_I$ = reset term in repeats per minute
T_D = rate term in minutes

1771-PD Algorithm

The equation for PID closed loop control is:

$$V_O = K_P(E) + K_I/(E)dt + (K_D)d(E)/dt + Bias$$

Where K_P = proportional gain
K_I = integral gain in inverse seconds
K_D = derivative gain in seconds

Comparison

The ISA standard algorithm contains dependent variables. When you change your controller gain (KC), you also change your integral and derivative values.

The 1771-PD algorithm contains independent variables. You adjust the proportional, integral, and derivative terms independently.

Word	ISA Algorithm	A-B Algorithm
W07 (W14)	Proportional Gain K_C (dimensionless)	Proportional Gain K_P (dimensionless)
W24(W44)	Reset Term $1/T_I$ repeats per minute)	Integral Gain K_I (inverse seconds)
W25(W45)	Rate Term T_D (minutes)	Derivative Gain K_D (seconds)

Conversion

Converts ISA standard values to 1771-PD values as follows:

$$K_P = K_C$$

$$K_I = \frac{K_P \ (\text{\# repeats per minute})}{60}$$

$$K_D = K_P(T_D)(60)$$

Example

If you desired ISA standard values are:

controller gain = $K_C = 1$
reset value = $1/T_I = 5$ repeats per minute
rate term = $T_D = 3$ minutes

convert them to 1771-PD values as follows:

proportional gain = $K_P = K_C = 1$
integral gain = $K_I = \frac{(1)(5)}{60} = 0.083$

derivative gain = $K_D = (1)(3)(60) = 180$

Insert the converted gain values into the 1771-PD algorithm as follows:

proportional gain word W07(W14) = 01.00
integral gain word W24(W44) = 0.083
derivative gain word W25(W45) = 18.00 x10

Selecting the Algorithm

You select the ISA or A-B algorithm using Bit 00 in control word W02 as follows:

- ISA algorithm: W02 B00 = 1
- A-B algorithm: W02 B00 = 0

Appendix F

Algorithm Flow Chart

Appendix F

Rockwell Automation

Allen-Bradley

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