PowerFlex 700S DriveLogix

Allen-Bradley

Application Guidline

Analog Input Response Time

Description

This document serves as a supplement to the PowerFlex 700S Users Manual (20D-UM001A-EN-P) addressing items specific to the PowerFlex 700S analog inputs. The purpose of this test was to measure the response time between a change of an analog speed reference and when a fluxed up motor reacted to that change on a PowerFlex 700S. Please refer to the Users Manual for details on the PF700S analog I/O wiring and setup.

Technical Information

Before taking the measurements, motor data was entered and an autotune was performed on the connected motor. The motor was unloaded.

Additionally, the following parameters were set:

- P89 [Spd Err Filt BW] = 0 Rad/Sec
- P90 [Spd Reg BW] = 40 Rad/Sec
- P151 [Logic Cmd Word] = 0000 0000 0000 0001 (Bit 0 was set to 1 to disable the speed ramp)

To measure the response time, an analog input was configured as the speed reference. The drive was started with a 0 RPM speed reference. A 0 to 10V supply was wired through a switch into the analog input. Then the time between a 0 to 10V step change on the analog input and the motor current to reach 2/3 of its peak was measured with an oscilloscope.

20 trials were performed with the following results:

- Average time = 2.2 ms
- Worst case response time = 3.4 ms

The response times can be broken down as follows:

Analog input delay time = 0.8 ms
VPL (velocity processor loop) time = 0.5 ms
Time to ramp Iq to 2/3 = remaining time

So the variable in the response time is the time to ramp Iq to 2/3. From our testing, we can see that P89 [Spd Err Filt BW] and P90 [Spd Reg BW] affect how fast the drive responds to a step change in the speed reference, and therefore how fast Iq is ramped up. Decreasing P354 [Iq Rate Limit] will tend to make the Iq ramp time longer. Setting P153 [Control Options] bit 11 will also make the Iq ramp time longer.