IEEE Industry Application Society
Annual Meeting
New Orleans, Louisiana, October 5-9, 1997

Modeling and Analysis of DC Link Bus Capacitor and Inductor Heating Effect on AC Drives (Part I)

Ajith. H. Wijenayake,* Dennis H. Braun,** Michael L. Gasperi,* Tom P. Gilmore,** Dan C. Pixler**

Rockwell Automation*
Adv. Tech Labs
1201 S. Second Street
Milwaukee, WI 53154
(414) 382-5798 382-2508

Rockwell Automation**
Standard Drives
West Enterprise Drive
Mequon, WI 53092
(414) 242-8292 242-8261 242-7096

ABSTRACT- ***The overall performance and efficiency of a voltage source inverter (VSI) can be improved by selecting a combination of DC link capacitance and DC link inductance based upon a weighted optimization criterion. Developments of semiconductor technology have enabled present semiconductor devices to operate with improved power losses, to a great extent. However, still there is a considerable amount of power loss in the DC link capacitor bank and DC link inductor. These loss components are normally ignored to a certain level in terms of design/efficiency optimization, in the design phase of the drive. Therefore, there are additional opportunities to optimize the design by selecting the capacitor/inductance combination for minimum power losses or for any other any other optimum such as size and weight or cost. This paper describes the modeling of the PWM AC drive, AC motor and special modeling of the DC bus capacitor and DC link inductor, using SABER simulator. The paper compares the Saber simulation results with the experimental data to verify the accuracy of the model, for given values of DC link inductance and bus capacitance, as the first step towards modeling the overall system for accurate prediction of the drive performance.***

1.0 INTRODUCTION

Modeling and simulations of power converter circuits have been an enormous aid in forecasting circuit performance and improving cycle time from circuit design to manufacturing by eliminating most of the prototype iterative testing needed.

Power semiconductor device modeling, as non ideal switches, is an essential part of such analysis, if realistic performance is to be predicted. In order to accomplish such performance prediction, the design engineer should be able to accurately model and simulate the entire drive/motor system. In such systems, the modeling of inverter power devices and motor can be accomplished within a reasonable accuracy.

The accurate modeling of capacitor and inductor, to reflect their actual performance and power losses, is difficult due to so many dependencies. In capacitor modeling, it is very important to include it's parasitic elements such as equivalent series resistance (ESR), and actual variation of capacitance, if correct performance over the life span is to be investigated. However, this is complicated by the fact that ESR, and actual capacitance are frequency, temperature and life time dependent [1].

Presently, the DC link inductor's function in the drive is to meet the input power factor and harmonics requirements. The value of this inductor can be selected to optimize power losses (i.e. capacitor losses, inductor copper losses and core losses), and hence the efficiency of the overall system. This necessitates an accurate inductor model which will represent the copper and core losses separately, as a function of core operating temperature flux density, current ,frequency (frequencies), and other physical parameters of the inductor.

Due to the complexity of the total VSI model with the nonlinear effects of the power semiconductor switches, the different time constants and dependencies of the power components such as the DC link inductance and DC bus capacitance, analysis of the detailed behavior at the system level as well as at the device level can be quite challenging.

Thermal management of the DC link inductance and DC bus capacitance is a major concern and must be included in the overall system model of the VSI.

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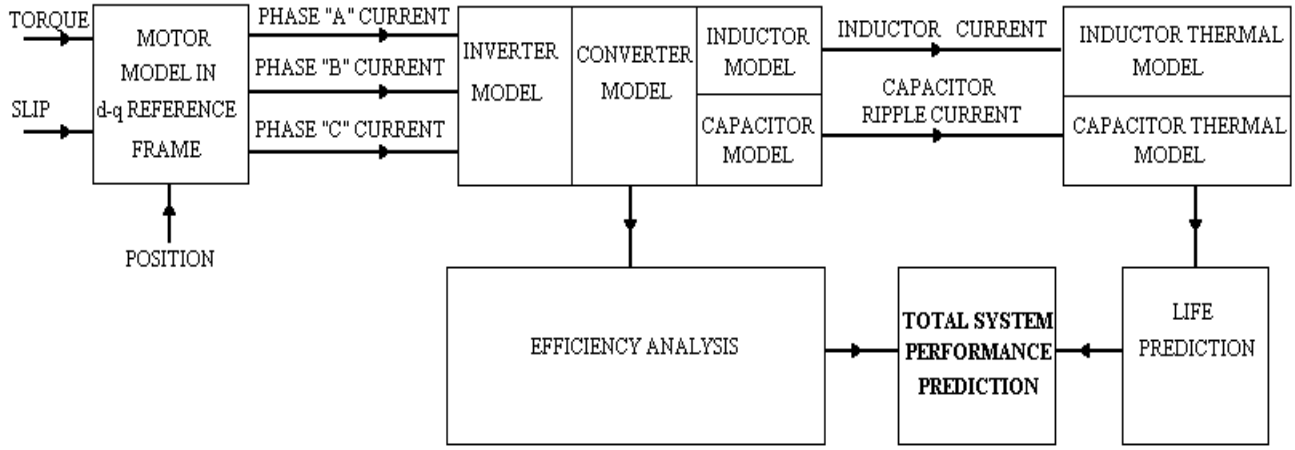

Figure 1. Block diagram of the modeling scheme.

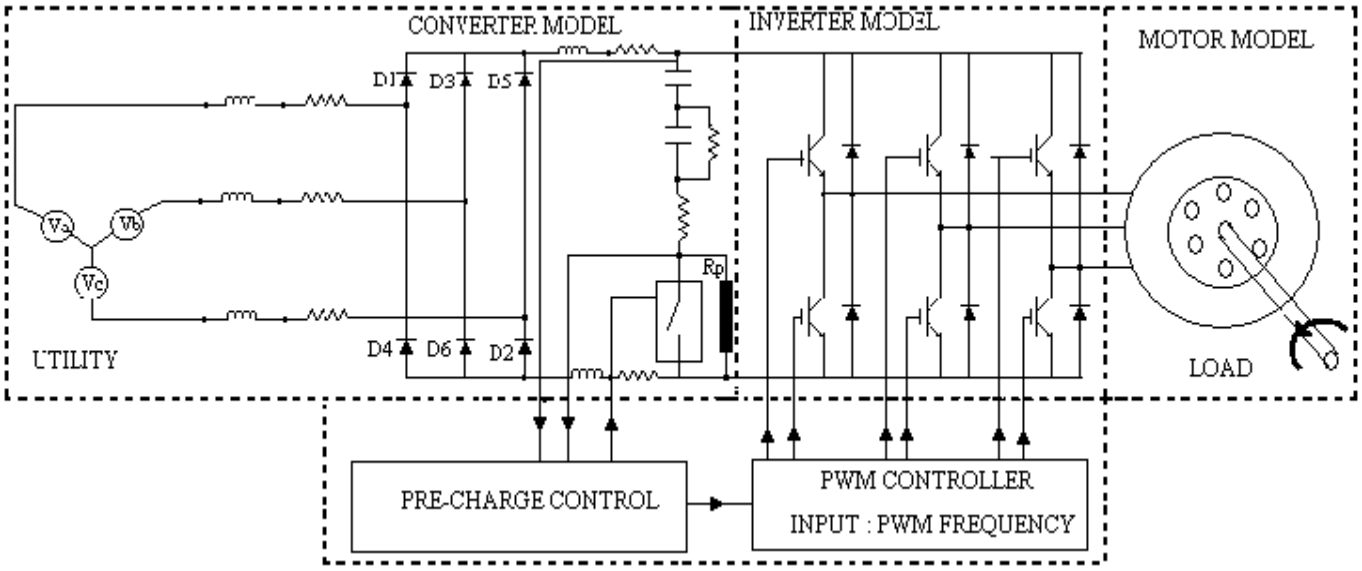

Figure 2. SABER system model for the adjustable speed drive system.

Most simulation programs, with integrated circuit emphasis, do not provide the capability to effectively analyze many of these aspects of power electronics systems. SABER, [2], a simulation package based on analog hardware descriptive language (AHDL) is well suited for such power electronic circuit simulations, due to its device modeling features as well as thermal modeling capabilities, and other functional features. SABER simulator is capable of simulating entire power electronics system in a single simulation environment, since it's thermal analysis capabilities can be readily incorporated into the overall analysis and design of the drive system. Figure 1 shows the block diagram of the modeling scheme required to analyze and predict the overall system performance.

2.0 MODELING OF THE ADJUSTABLE SPEED DRIVE SYSTEM

The SABER system model for the drive system is a combination of three system modules and the load profile. The three system modules include a converter model with pre-charge control ,an IGBT inverter model with PWM controller, and induction motor model.

A. Modeling of DC Bus Capacitor

The DC bus capacitor bank is made up of normally, eighteen, high ripple current rated, aluminum electrolytic capacitors. In

the modeling of an electrolytic capacitor which contains only a single frequency ripple current component, the ESR can be adjusted by using a multiplier factor which accounts for the effect of frequency on dielectric resistance. In a motor drive, the capacitor ripple current consists of many frequency components, and therefore each frequency component requires its own ESR model. Figure 3 and Figure 4 show the actual variation of capacitance and ESR over the expected life of 5000 hours, for a 4600 uF capacitor.

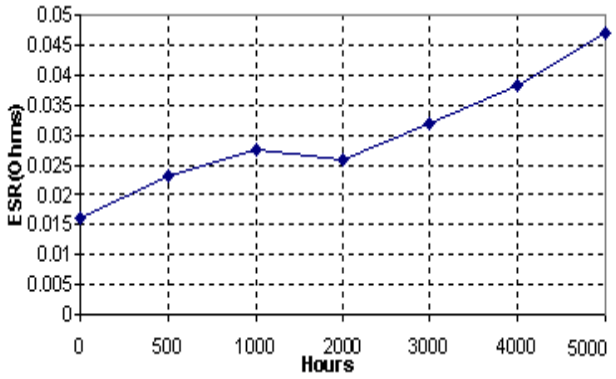

Figure 3. Variation of ESR over expected life (Measured).

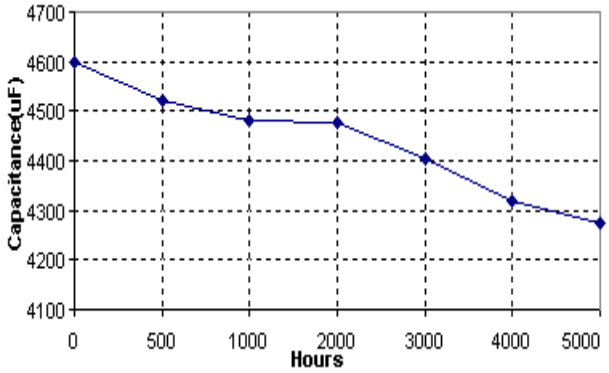

Figure 4. Variation of capacitance over expected life (Measured).

Over the measured period of time the capacitance decreased by about 7%, and ESR increased by 196% due to vaporization of electrolyte through the end seal [4]. ESR is also inversely proportional to operating temperature and this variation has been modeled by equation (1), in [5]. The parameter variations of the capacitor make it very difficult to develop a dynamic ESR model for a capacitor. The constants D, Y, and F in equation (1) can be found by using experimental data for a given capacitor [5].

$$\frac{ESR(T_1)}{ESR(T_0)} = D + Ye^{-(T_1-T_0)/F} \quad \ldots\ldots\ldots\ldots\ldots\ldots(1)$$

Figure 5 shows an enhanced ESR model for an aluminum electrolytic capacitor [6]. Manufacturer's data can be used to obtain the values of R_1, R_0 , C_2, and R_2 [6]. This model, combined with equation (2) and ESR life test data can be used to obtain the heat dissipation in the capacitor bank, with reasonable accuracy, for a given operating condition. SABER's thermal modeling capabilities can be used to obtain an accurate dynamic thermal ESR model of the dc bus capacitor bank.

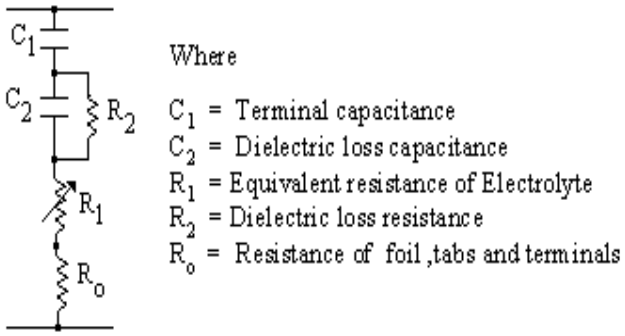

Figure 5. Dynamic ESR model for an electrolytic capacitor.

Actual ESR variation with temperature and frequency was measured for a 4600 uF , 400 V dc bus capacitor, and the results are shown in Figure 6.

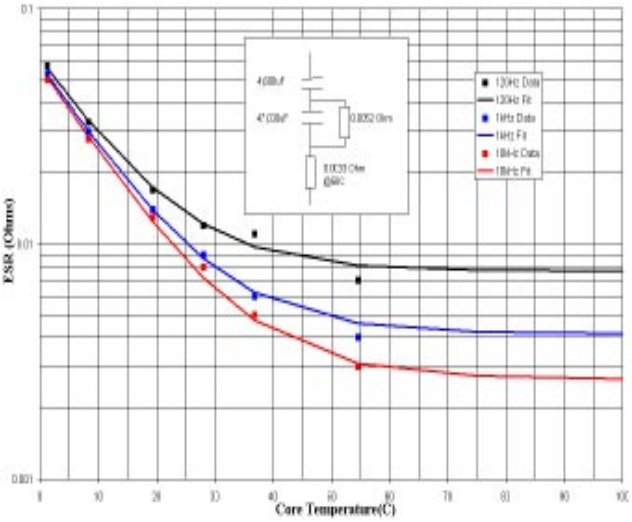

Figure 6. ESR variation with temperature and frequency.

The corresponding equation for the ESR variation with temperature was obtained using the test data, and is shown in equation (2). This equation can be implemented in SABER capacitor thermal model to reflect the actual ESR variation with the temperature.

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$$R_1(T) = 0.00265 + 0.00492e^{(300-T)/F} \quad \text{.....(2)}$$

B. Modeling of DC Link Inductor

The simple ESR model based on winding resistance of the inductor is not accurate enough for realistic performance evaluation. At high current level and high frequencies, the core loss components become dominant. This effect should be included in the equivalent circuit series, R_c in addition to winding resistance, R_w. The equivalent circuit is shown in Figure 7 , where R_w, R_c, C represent the inductor winding resistance, equivalent magnetic core loss resistance and inductor self-capacitance respectively.

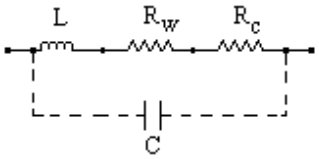

Figure 7. Equivalent circuit for the DC link inductor.

Over the normal operation frequency range of the inductor, the capacitive component can be neglected. The R_c component is a non linear function of frequency, current and operating temperature of the inductor [4]. These components can be found by performing steady state thermal/power loss measurements of the inductor, over the operating current and frequency range. Equation (3) [4] can also be used to determine the core loss and hence the equivalent magnetic core loss resistance for a given operating condition of the inductor.

$$P_{Fe} = V_e C_m f_e^{1.6} \left(\frac{LI_{max}}{NA_e} \right)^{2.5} \left(C_T - C_{T1}T + C_{T2}T^2 \right) \ldots (3)$$

Where

P_{fe}= Core Losses N= no. of turns

V_e= Core volume A_e= Effective core area

C_m= Coefficient depending on core material

f_e = Frequency, L = Inductance

C_T, C_{T1}, C_{T2} = Constants (found from experimental data)

I_{max}= Max. current T= Core temperature

An alternative approach to determine core losses of the inductor is to use SABER non linear inductor model. This model's template building requires magnetic and physical parameters of the inductor for calculating the copper losses and core losses separately.

3.0 SIMULATION RESULTS

The drive system which consist of a 500 HP induction motor, a 450 HP PWM IGBT inverter with diode front end rectifier, a DC bus capacitor bank, positive and negative bus DC link inductors, was simulated for different DC bus capacitor bank and link inductor values. The capacitance value chosen were 13,800uF, 20,700uF, 27,600uF. These values were corresponding to 12, 18, and 24 cans of 4600uF capacitors, respectively. The DC link inductor values chosen were 53.5uH, 107uH, and 214uH. SABER simulator's "vary" command can be used within capacitance and inductance loops to run the simulations for both parametric variation analysis, for one simulation frequency at rated current. SABER simulator's graphical waveform analyzer, SCOPE, has the capability of showing all nine data points for a signal, in the same graph . Figure 8 shows the simulated data with simple ESR capacitor model and enhanced ESR capacitor model which takes the ESR variation with temperature and frequency, into account.

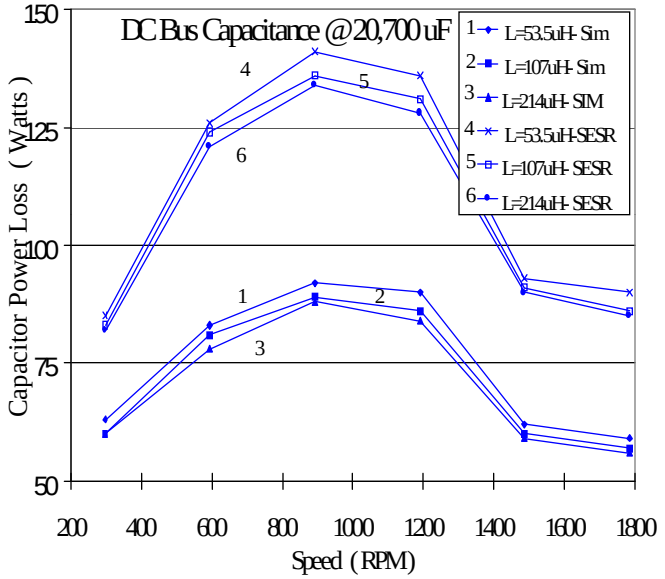

Figure 8. Capacitor power loss with simple ESR model and enhanced ESR model (simulated data).

Figure 8 shows that the power loss in the capacitor is reduced by about 25-30% if the enhanced ESR model is employed in the simulation. This implies that the capacitor bank can handle more ripple current for a given steady state core temperature or, the capacitance can be reduced further for a given load current to operate at the same steady state core temperature.

4.0 EXPERIMENTAL RESULTS

The experimental set up used for the verification of the simulation results and the accuracy of the system model, consists of a 450 HP PWM IGBT inverter, a front end rectifier supplied by a 460Volts three phase supply, 20,700uF capacitor bank, and a 500 HP induction motor. Three values of total DC link inductance chosen were 53.5uH, 107uH, and 214uH. The motor was operated at the rated current which was at 532 Amps. The

steady state core temperature of the capacitors was kept at 55 C. However, the accurate measurement of the link power loss was not possible due to very low value of the power loss and the disturbance signals due to common mode noise. Figure 9 shows the comparison between the measured power loss of the capacitor bank and the power loss obtained using simple ESR model and enhanced ESR model. The measured power loss data agree very closely with that of the simulated data of the enhanced ESR capacitor model.

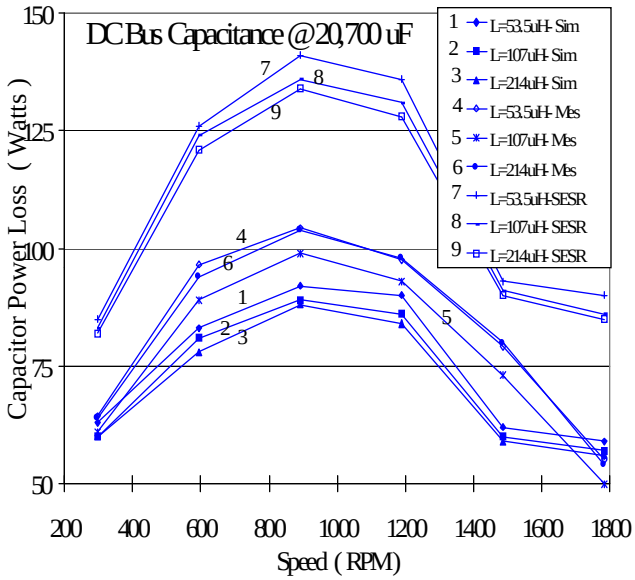

Figure 9. Comparison between measured and simulated power losses for the DC bus capacitor bank.

Figure 10 shows the total power dissipation in the DC link inductor and DC link bus capacitor bank. In calculating DC link inductor total losses the core losses were neglected due to inaccurate measurements. Therefore, only the copper losses are counted towards the total losses of the inductor. The modeling of the inductor in SABER was also not possible due to unavailability of the physical and magnetic parameters of the inductor, at this instant. This issue will be addressed in the future work.

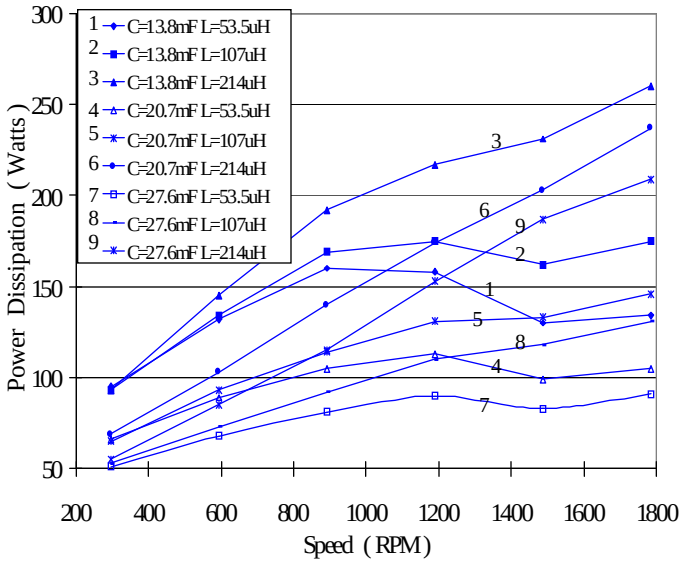

Figure 10. Total power dissipation in the DC link components for different combination of DC link component values.

Figure 10 clearly indicates that the total power dissipation of the DC link components has a maximum value for certain combination of DC link inductor and DC bus capacitor values. This peak occurs around 40 Hz, due to pulse dropping of the PWM operation. However, the capacitor loss peaks around 30 Hz as shown in figure 9. As seen by the simulation data at higher DC link inductance values, and at higher frequencies, the power dissipation of the inductor is the dominating part of the total loss component. Therefore, total power loss increases as the operation frequency is increased. Figure 11 shows the comparison between the measured total power loss data and that of the simulated data.

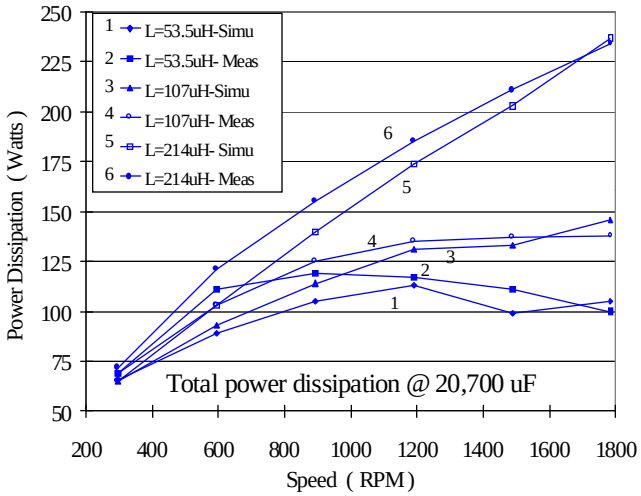

Figure 11. Comparison between measured and simulated total power loss of the DC link components.

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It is clear that the lowest total power dissipation occurs at the highest value of bus capacitance and the lowest value of link inductance. This combination is optimum in terms of energy losses. However this may not be the optimum design selections with respect to other performance parameters, such as the cost, size, and the total harmonics distortions. A simple cost analysis is given below for different combination

5.0 DC LINK COMPONENTS COST ANALYSIS FOR DIFFERENT VALUES OF CAPACITANCE AND INDUCTANCE COMBINATIONS

Cost analysis for this paper is based upon per unit linearization costs for the DC bus capacitor and DC link inductor chosen as nominal values.

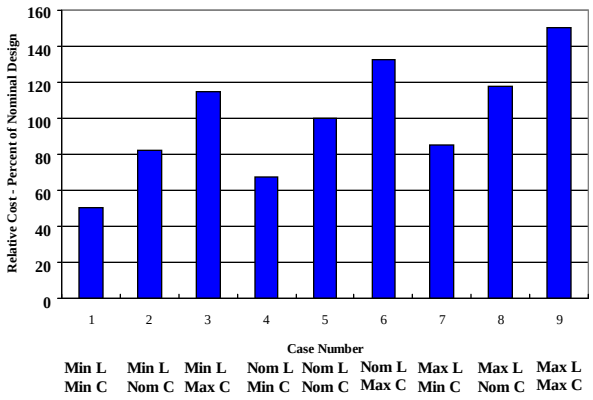

Figure 12. Cost Comparison of DC Link Inductor & DC Bus Capacitor Components.

Referring to Figure 12, the minimum cost function as case # 1 of minimum inductance and minimum capacitance is the obvious choice, as is the worst case of both maximum values. Of particular interest is case #3, of minimum inductance and maximum capacitance since this is the case that produces maximum efficiency. This case results in a relative cost increase of 14 percent higher than nominal cost. Since no total cost analysis of the drive product is included, further detailed work would be required to produce conclusive impact on the product considering weighted optimization of one index to another.

6.0 CONCLUSIONS

This paper has successfully produced a SABER simulation model that accurately produces power dissipation of the DC link components. The effort has provided special models of these DC link components which will serve as a template for further detailed modeling work and performance analysis in support of power structure research and development.

As a further benefit this work has provided insight into complicated methods of proper instrumentation of power waveforms for the power structure.

Future work will include further testing to obtain the link power losses accurately, and input current spectrum for determining the total harmonic distortion (THD); total demand distortion (TDD); and the power factor for different values of capacitor and inductor combinations. This will allow the designer to look at the drive performance in terms of power quality related issues. In determining distortion, it is TDD rather than THD that is the more important quantity to calculate, since TDD is the based on the rated load current and not on the operating point of the load.

The inductor thermal testing should also be completed in order to model the inductor for separating the copper and core losses. The non-linear inductor model for the DC link inductor in SABER will also be developed to provide a more accurate model of the actual system.

7.0 ACKNOWLEDGEMENTS

We would like to thank Steve Swanson at Analogy, Inc. for helping to develop the SABER drive system model used in the simulations and Paul LeMay for his help during the actual testing and data collection.

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