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On the Loading of Power Modules in a Three Phase Voltage Source Converter

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ABSTRACT -- The loading of free wheel diodes (FWD) and IGBTs in the power modules of a Voltage Source Converter (VSC) are investigated. In converter duty, the FWD is utilized more then the IGBT. Presently, most FWD's in power modules are optimized for inverter duty. This practice tends to undersize the FWD from a converter viewpoint. This design philosophy is examined in the paper. For this purpose, the original dynamic thermal model of IGBT and FWD were developed. Model parameters were identified from the manufacturers catalogue data. A mathematical model of the entire VSC was developed to compute current, voltage, power and thermal conditions for the power module and other components in converter operation.

I. INTRODUCTION

The power module of Voltage Source Inverter (VSI) in an electric drive consists an IGBT with an anti-parallel free wheel diode (FWD). The module is highly optimized for inverter duty applications with an assumption that drive operates from moderately low to higher speed ranges of the motor and thus with a modulation index greater than 0.5. In such a duty, dominant loading is on the IGBT. The loading of FWD is not critical. To optimize the price/performance ratio, power module manufactures increase the forward voltage drop on the FWD and it is typically in the range of 2.0 to 2.5 volts. Furthermore, the thermal resistance, junction - case, of the FWD is usually double in comparison to the thermal resistance of the IGBT. This occurs since the ratio of the FWD to the IGBT die size varies from about 0.4 to 0.6 depending on power module manufacturer. Such an "optimization" created problems and failures of FWD's at stalled rotor or at very low motor speeds. These operating conditions represent a small segment of inverter applications and hence a small segment the power module market. This provides sound economical justification to optimize the power module in this manner.

On the other hand, the situation is totally opposite with three phase Voltage Source Converters (VSC), often referred in literature as a three phase synchronous rectifiers. VSC's are used as the "front end" of the drives or as a part of an integrated drive (consisting of a VSC and a VSI in the same package sharing common DC capacitor bank). The VSC in Fig. 1, is able to maintain constant DC bus voltage, sinusoidal input current and unity power factor [4]. Its control is similar to the vector control of the induction motor with two main distinctions: (a) speed feedback is replaced with output dc voltage feedback u_{dc} and (b) instead of position of rotor flux, the position of utility voltage space vector θ is used as the reference angle in all the blocks for reference frames transformations. Output of a voltage regulator U_reg creates active q current component reference i_{q_c} for the synchronous reference current regulator Iq_reg. The another current reference i_{d_c} is used for the control of reactive current. It is set to zero to maintain unity power factor. The outputs of digital synchronous reference frame current regulators Iq_reg and

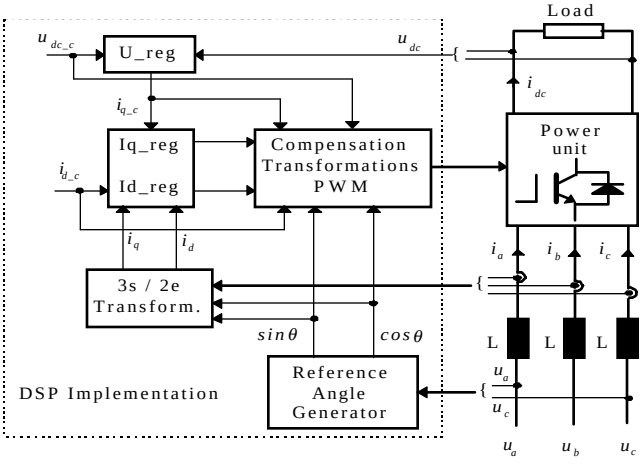

Figure 1 VSC Block Diagram

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Id_reg are further processed in Transformation - Compensation - PWM block to create gating pulses for the IGBT bridge in the power unit.

In VSC applications, the direction of energy flow through power devices is opposite to the direction of energy flow in the VSI. Since the VSC operates mostly in motoring mode, the majority of current loading in the power module is on the FWD's which supply energy to the inverter. The IGBT devices are fully loaded only for short time during regenerating thus having a very small duty cycle.

This paper examines the current "optimization" practice of power module designs and points out the differences in loading of power modules in converter and inverter applications. It provides the original dynamic thermal model of IGBT and FWD and a method to identify the model parameters from manufacture's data. The mathematical model of the entire VSC was developed which enabled the computation of instantaneous values of current, voltages and power losses during every PWM switching period. The temperature variations, within the resolution of PWM carrier period, of the FWD and IGBT junctions were computed as a function of load. The influence of thermal variations on life expectancy of the devices was analyzed. In the addition to the power module, the loading on the other power circuit components namely capacitor bank in DC link and fuse are analyzed.

II. DYNAMIC THERMAL MODEL OF POWER DEVICE

The thermal impedance, junction - case, model of semiconductor devices was developed in [1] to [3] and is shown in Fig. 2(a). Using partial fraction expansion, (the ratio of two polynomials) and the impedance equation from the schematic diagram in Fig. 2(a), the equivalent diagram in Fig. 2(b) was obtained :

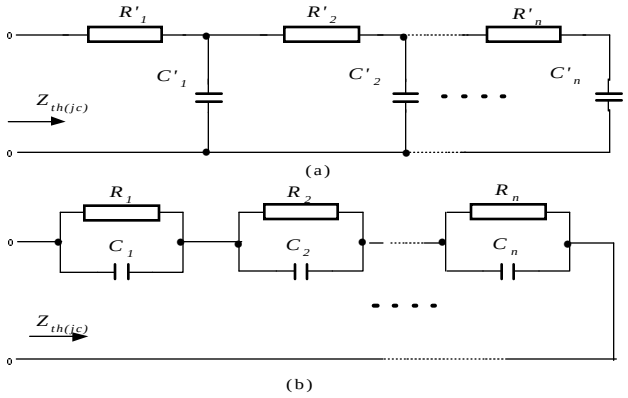

Figure 2 Equivalent diagram of thermal impedance, j-c, of a semiconductor device "transmission line" **(a)** and series connection of RC elements **(b)**

$$Z_{th(j-c)}(s) = \frac{R_1}{1+s\tau_1} + \frac{R_2}{1+s\tau_2} + ... + \frac{R_n}{1+s\tau_n} \quad (1)$$

where $\tau_i = R_i C_i, \quad i = 1,...n$.

The total steady state thermal resistance, junction -case $R_{th(j-c)}$ equals to the sum of the resistors R_1 to R_n i.e.:

$$R_{th(j-c)} = \sum_{i=1}^{n} R_i \quad (2)$$

The manufacturer's usually define transient thermal impedance as a function of time. Their definition corresponds to the temperature change on the junction when step of "unity" power dissipation is applied. In our case, it would correspond to the multiplication of (1), with Heviside's unity step function and then transforming it in the time domain by Laplace transformation. Thus the time domain thermal impedance, normalized to the thermal resistance $R_{th(j-c)}$ is obtained:

$$z_{th(j-c)}(t) = r_1(1+e^{t/\tau_1}) + r_2(1+e^{t/\tau_2}) + ... + r_n(1+e^{t/\tau_n}) \quad (3)$$

where

$$r_i = R_i / R_{th(j-c)}; \; i = 1,...n \quad (4)$$

The parameters $r_i, \tau_i; \; i = 1,...n$ in (3) were identified using LMS algorithm with the target function

$$F = F_p + \sum_{k=1}^{m} [z_{th(j-c)}(t_k) - z^{md}_{th(j-c)}(t_k)]^2 \quad (5)$$

where F_p is a quadratic penalty function which keeps the parameters within specified limits, m is a number of points of approximation, $z_{th(j-c)}(t_k)$ is the thermal impedance calculated from (3) and $z^{md}_{th(j-c)}(t_k)$ is the thermal impedance from manufacturer data, both at the instant t_k . It was found

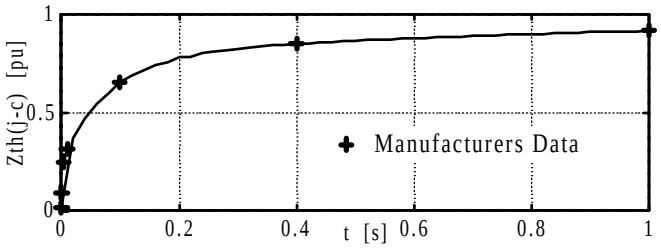

Figure 3 Manufacturers thermal impedance data, (+), with the approximation from eq (3)

that the approximation of the thermal impedance with equation (3), by using three terms, n=3, gives an acceptable fit. The

Table 1 Parameters of eq (4) for the thermal impedance of the FWD and IGBT of a 600 A, 1200 V power module, time constants are in seconds

	r_1	r_2	r_3	τ_1	τ_2	τ_3
Diode	0.2491	0.5315	0.2194	0.0024	0.0797	0.9901
IGBT	0.2629	0.3892	0.3479	0.0044	0.0736	1.1873

quality of approximation is illustrated in Fig. 3 for a FWD in a 600 Amp, 1200 Volt IGBT power module. Table 1 lists the parameters for the FWD and IGBT device from the same 1200V, 600A module. Note that the shortest time constant τ_1 in Table 1 is smaller then 5 ms and the corresponding thermal resistance is about 25% of the total steady state resistance. This indicates that the junction temperature will follow variations in power dissipation at a 50/60 Hz cycle rate.

III. LOADING OF A DIODE VS. LOADING OF IGBT

Figure 4 shows the schematic diagram of a VSC power circuit. The VSC maintains constant bus voltage during motoring and regenerating and regulates U_{dc} to 10 to 15% higher [4] in value then the peak of line to line voltage (i.e. the output value of the FWD bridge U_{db}) i.e.

$$U_{dc} = (1.1 \; to \; 1.5)U_{db}; \quad U_{db} \approx \sqrt{2}\,U_{ll}, \tag{6}$$

where U_{ll} is line to line voltage.

The analysis of duty cycle and power conditions in power circuit of a VSC was done in [5] with the assumption that the neutral O_u of utility and center point of the capacitor bank O_c are at the same potential. This assumption is true only on a locally average basis over carrier period for symmetrical sinusoidal triangle comparison PWM. However, frequently used space vector, third harmonic and discontinuous PWM

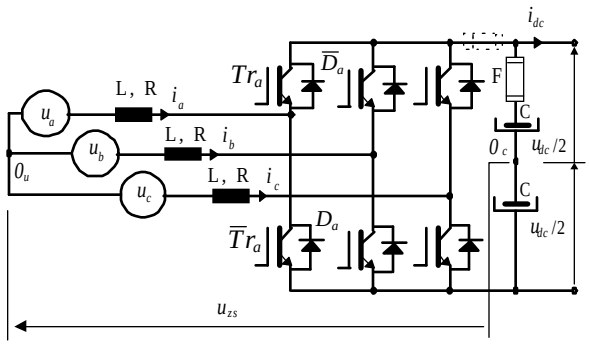

Figure 4 VSC Power Circuit Diagram

methods add zero sequence component u^*_{zs} to the original modulation waveforms $u^*_{abc} \in \{u^*_a, u^*_b, u^*_c\}$, [6]:

$$u^{**}_{abc} = u^*_{abc} + u^*_{zs}, \tag{7}$$

$$u^*_{zs} = -[(1-2k_0) + u^*_{\max} + (1-k_0)u^*_{\min}] \tag{8}$$

where $u^{**}_{abc} \in \{u^{**}_a, u^{**}_b, u^{**}_c\}$ is a new set of modulation waveforms at the input of PWM, $u^*_{\max} = \max\{u^*_a, u^*_b, u^*_c\}$ and $u^*_{\min} = \min\{u^*_a, u^*_b, u^*_c\}$. Factor $0 \le k_0 \le 1$ is a ratio of duration of application of zero state vector V7 and combined duration of applications of zero state vectors V7 and V0 within a carrier period, [6].

The addition of u^*_{zs} to the set of modulation reference voltages u^*_{abc} results in a zero sequence voltage u_{zs} between points O_u and O_c. Locally averaged value of zero sequence voltage $\overline{u}_{zs}$ over carrier period T_c

$$\overline{u}_{zs} = \frac{1}{T_c}\int_0^{T_c} u_{zs}\,dt \tag{9}$$

for the non-saturated PWM modulator, (9) is proportional to u^*_{zs}:

$$\overline{u}_{zs} = K_{PWM}\,u^*_{zs} \tag{10}$$

where K_{PWM} is the gain of the PWM modulator.

Using (7) to (9) the analysis of current and voltage conditions in power circuit of a VSC from [5] can be expanded from sinusoidal symmetrical PWM to the other PWM methods which introduce zero sequence in order to increase linearity and utilization of dc bus voltage.

The method to determine the duty cycle and loading of the IGBT and the FWD with zero sequence voltage present will be illustrated with the phase *a* VSC input shown in Fig. 4. During motoring operation of the VSC, the energy will flow from the utility towards the dc bank, and during positive half cycle of u_a, the IGBT device $\overline{T}r_a$, conducts applying the voltage to the inductance L:

$$\overline{u}_L(\overline{T}r_a) = 0.5u_{dc} + \overline{u}_a + \overline{u}_{zs} \tag{11}$$

where a bar over a later *u* indicates locally average value.

After $\overline{T}r_a$ is turned off, current commutes to the $\overline{D}_a$ and energy is transferred from the line reactors to the dc bus capacitors,

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i.e. fly - back operation. During conduction of $\overline{D}_a$ the voltage on inductance L is substantially smaller then during conduction of the transistor:

$$\overline{u}_L(\overline{D}_a) = -0.5u_{dc} + \overline{u}_a + \overline{u}_{zs} \tag{12}$$

The duty cycles for the diode d_D and IGBT d_{IGBT} follow from the required equilibrium of volt seconds when voltages (11) and (12) are applied on L:

$$d_D = \frac{0.5u_{dc} + \overline{u}_a + \overline{u}_{zs}}{u_{dc}} \tag{13}$$

$$d_{IGBT} = \frac{0.5u_{dc} - (\overline{u}_a + \overline{u}_{zs})}{u_{dc}} \tag{14}$$

Note that during motoring operation of VSC, d_D is much higher then d_{IGBT} and consequently, the period of conduction of the FWD's is substantially longer then the period of conduction of the IGBT devices. Therefore, FWD's take more current during motoring then the IGBT. The situation is opposite during regeneration when the bulk of the load current is taken by the IGBT devices. However, motoring is predominant mode of operation of the drive and current loading of diodes during motoring becomes critical.

IV. MATHEMATICAL MODEL OF A VSC

The mathematical model of the complete VSC (power and control section [7]) was built, for more precise evaluation of loading of power devices and variations of temperature within a period of fundamental cycle (50/60 Hz). Operation with constant PWM frequency was assumed. Figure 5 shows a Matlab model of the 'local averager' which enables calculation of average value of signal over "hold" time T_h. Note that of the output of averager is obtained with a hold *delay* of T_h. The averager was used for evaluating the highly discontinuous variables like current through power devices over a carrier period or fundamental period.

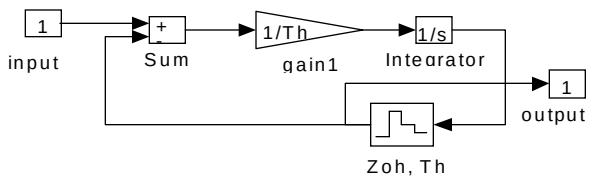

Figure 5 Block Diagram of Signal Averager

The quasi instantaneous loses on IGBT p_{IGBT} ,and FWD p_D, were determined as

$$p_{IGBT} = i_{IGBT}\ u_{ce(sat)}(i_{IGBT}) + \\ + [E_{SW(on)}(i_{IGBT}) + E_{SW(off)}(i_{IGBT})]\, f_{PWM} \tag{14}$$

$$p_D = i_D\ u_{ak}(i_D) + E_{rr}(i_D)\, f_{PWM} \tag{15}$$

where i_{IGBT} and $u_{ce(sat)}$ are current and voltage of the IGBT during conduction, i_D and u_{ak} are current and voltage of the FWD during conduction. E_{SW} are switching energy losses of the IGBT and E_{rr} are energy recovery loses of the FWD, they were averaged over a carrier period, $T_c=1/f_{PWM}$, within which the switching happened. Where, f_{PWM} , is the PWM switching frequency. Note that in (14) and (15) voltage and energy losses are similar to those developed in [8] except that they are expressed as functions of instantaneous value of current. Their dependence on current was implemented by look - up tables.

V. CONDITIONS IN A VSC POWER STRUCTURE

Due to the tight packaging and requirements on small stray inductance's, it is hard and often impossible to measure currents through component in power structures of converters or inverters. Very often, simulation is the only tool for the analysis of current and power conditions in these mechanically tightly packaged power structures. Figure 6 shows the results of simulation; bus voltage, phase voltage current and locally averaged currents (over PWM period) of the IGBT and FWD in a 125 HP VSC during motoring (0 to 0.05 seconds) and regenerating (0.05 to 0.10 seconds). The FWD and IGBT currents in Fig. 6 were obtained at the output of averager with T_h equal to a PWM period. Note that almost all the line current goes through FWD during motoring and loading of the IGBT is about 10 to 15%, as expected from by (13) and (14). During regenerating, the situation is opposite, almost all the current goes through IGBT with small loading on the FWD.

Evidently, a power module optimized for VSC applications should have increased current carrying capabilities for the FWD and smaller current capabilities for the IGBT. Therefore, the optimization practice of power module for an inverter, when used for VSC type of applications, should be reexamined. However, if the VSC power structure is employed only as a regenerative brake to return energy to the utility, then the power module designed for inverter or drive type applications is optimal since the regenerative brake is typically sized for only a percentage of the drive rating.

The primary function of fuse F in Fig. 4 is to protect rupture of the power module in the case of failure by limiting the energy from the capacitor bank.

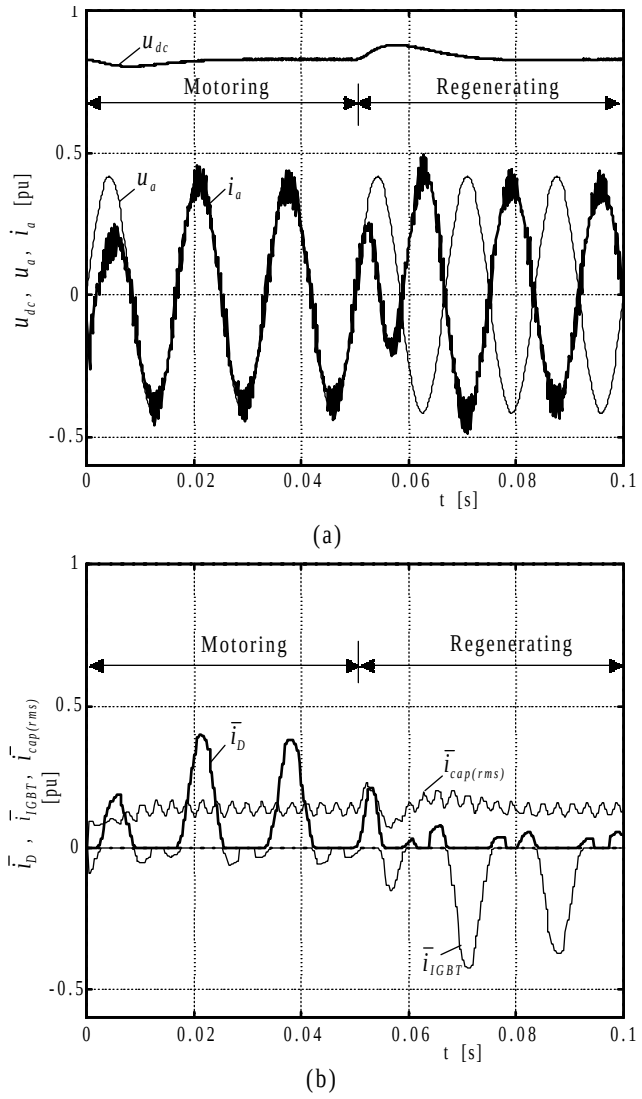

Figure 6 Loading of devices in power circuit of a VSC during motoring and regenerating; **(a)** dc bus voltage $u_{dc,}$ phase *a* voltage u_a and current i_a and **(b)** currents locally averaged over carrier period of: IGBT $\bar{i}_{IGBT}$, diode $\bar{i}_D$ and RMS capacitor current $\bar{i}_{cap(rms)}$. Base value of voltage and current are 903V and 660A respectively.

There are two main but opposing requirements governing selecting of this fuse. The fuse should have current carrying capability large enough to handle the rated load and any overload current requirements and on the other hand, small enough I^2t to avoid rupture of the failed IGBT module. "Premature" failure of the undersized fuse causes voltage break down and failure of power module. This occurs if the fuse opens prematurely and trapped inductive energy in the load and parasitics manifests itself as a high transient voltage since the current path is opened by the failed fuse. The nature of the VSC topology prohibits the traditional free wheel diode connected anti-parallel to the fuse as in the normal inverter configuration. The fuse selection is particularly troublesome due to the fatigue in dynamic applications with frequent overloads which are typical for VSC applications.

To reduce current through fuse, the fuse should be connected in series with capacitor as shown with solid line in Fig. 4. In this case, the fuse is loaded only with capacitor current. The position of the fuse shown with doted line in Fig. 4 is inferior because the fuse is burdened with load and capacitor current which makes selection of fuse with small I^2t difficult. The wave form of the RMS capacitor current calculated over the carrier period is shown in Fig. 6(b). The RMS capacitor current is relatively small, only about 25% of dc load current. The proposed dc bus fuse location implies that the upstream ac mains fuses to the VSC be appropriately sized and specified. They should be fast acting power semiconductor type fuses.

Figure 7(a) shows the dissipated power of the FWD and IGBT devices in the VSC power circuit during motoring operation. Values averaged over periods of carrier frequency and period of the fundamental are shown. Note that values averaged over period of fundamental (marked with a bar above symbol) are shifted right - delayed for sample and hold period, T_h which is equal to the fundamental period. However, this delay is not noticeable on waveforms obtained when averaging over short carrier period, $T_h = T_c$, because of the relatively high 5KHz PWM carrier frequency. The discontinuous PWM method from [4] which stops switching of IGBT for approximately 60 degrees was used. The discontinuity when switching is stopped is visible in losses on IGBT device p_{IGBT}.

Figure 7(b) shows FWD and IGBT junction temperatures. Note that pulsation of FWD junction temperature T_{jc_D} are about 8 ^oC. The frequency of the pulsation's is equal to the frequency of utility system. According to the manufacturing data, temperature variations smaller then 30 ^oC do not fatigue devices within the power module. Temperatures $\bar{T}_{jc\_D}$ and $\bar{T}_{jc\_IGBT}$ were computed using steady state thermal resistances junction - case and locally averaged dissipation over fundamental period. They are approximate steady state junction temperatures. The temperature increase, junction – case, on the FWD at rated load, is only 19 ^oC. This confirms that in this particular case, the inverter duty FWD will operate reliably in the converter duty application.

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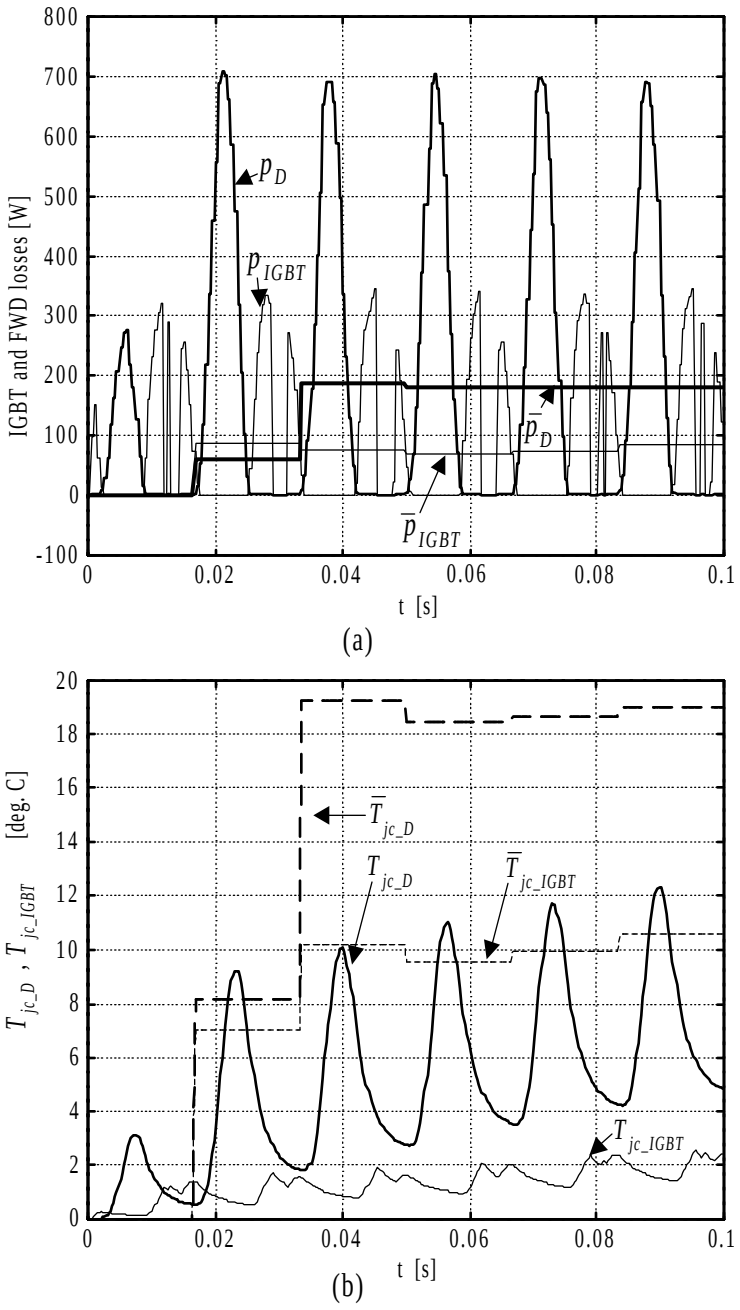

Figure 7 (a) dissipation on diode p_D and IGBT p_{IGBT} averaged over carrier period and dissipation on the same components $\overline{p}_D$ and $\overline{p}_{IGBT}$ averaged over fundamental period and **(b)** temperatures junction - case on diode and IGBT

VI. CONCLUSION

Power modules in converters applications have opposite modes of operation than modules in inverter applications, i.e., the FWD's are more heavily loaded than the IGBT devices. Since the standard power modules are optimized for inverter applications, the FWD's may be overloaded for converter applications and de-rating should be done to achieve reliable operation. For proper sizing of the devices, a precise thermal impedance model was developed. A third order thermal impedance model provided a good match with manufacturer's data. The model of the complete converter, together with a model of transient thermal impedance was developed and used for analysis of current, voltage, power and thermal condition in a VSC power structure. The variations of junction temperature on the IGBT and FWD vary from 2 to 8 ^{o}C and repeat at the utility frequency of 50/60 Hz at rated load conditions. In the particular case analyzed, a FWD from a 600A, 1200V IGBT power module optimized for inverter - drive duty application, proved to be able to operate satisfactory in VSC duty type of applications. Finally, a preferred location of the dc bus fuse has been defined. It is in series with the dc bus capacitors and not in the traditional inverter location, i.e., in series with the dc bus load.

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