

DMC ANALOG INPUT/OUTPUT

3100-AIO SERIES A

DESCRIPTION

3100-AIO (AIO86-8/4) provides 8 differential selectable - range analog inputs and 4 analog voltage/current outputs with 12-bit D/A conversion precision. 16 Device addresses are reserved by the board. Both the input and output analog signals are isolated channel specifically by an analog isolation unit.

INDICATORS

None

ASSOCIATED FUNCTIONAL BLOCKS

AIINI
AI
AOINI
AO

SPECIFICATIONS

Location:	CPU or I/O rack
Power Requirements:	5V @ .3 A., 15V @ .17A, -15V @ .17A
Environment:	Temperature: 0 to 50°C Humidity: 5 to 95%

SELECTIONS

Device Address (S1)

CONNECTIONS AND ASSOCIATED PRODUCTS

3130-UT
3130-AI

Switch Locations and Settings

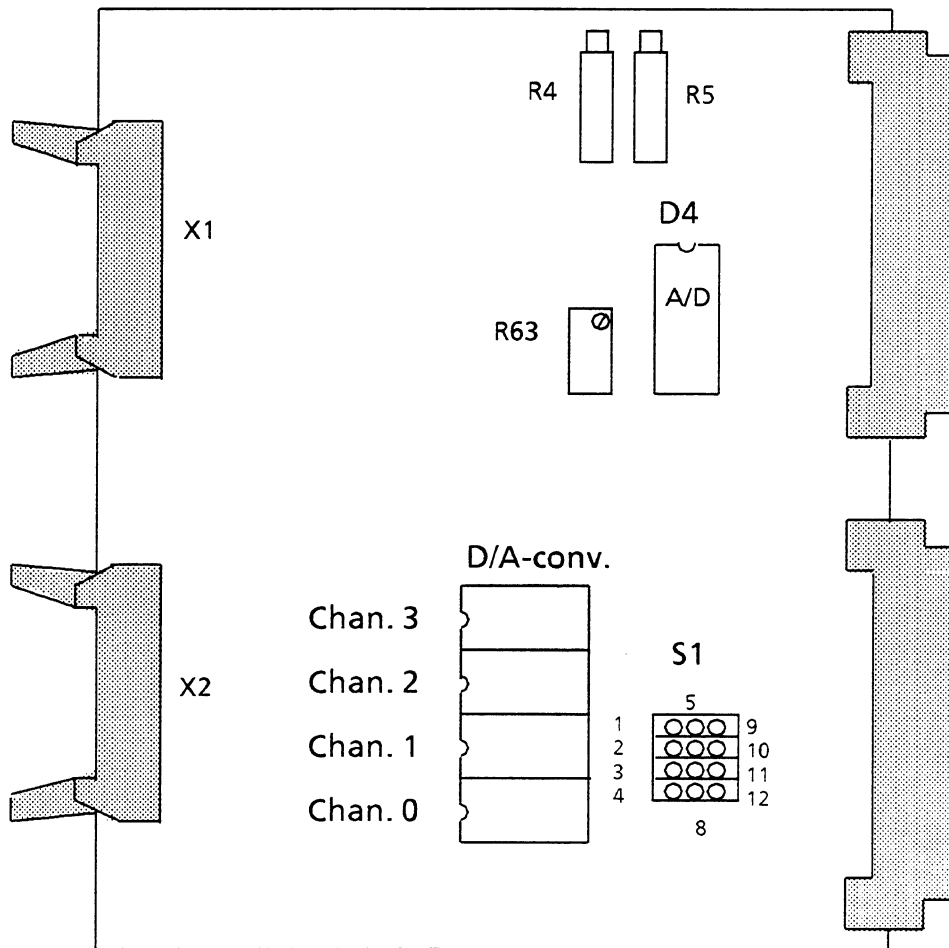


Figure 1. Address Selection Jumpers and Switch Locations on the 3100-AIO Board

Table 1. S1 Switch Settings

Hex Weight	80	40	20	10	8	4	2	1
Logic 0	5-9	6-10	7-11	8-12	X	X	X	X
Logic 1	1-5	2-6	3-7	4-8	X	X	X	X

Process Connection

Terminal strip boards 3130-AI and 3130-UT are necessary for process interconnection. The analog inputs and current source outputs of the 3100-AIO board are grouped together on a 40 pin flat cable. The 40 pole flat cable is connected to the X1 (upper) connector on the 3130-AI board (Figure 2) The analog outputs also use a 40 pole flat cable that runs from the X2 connector on the board to the upper connector on terminal strip board 3130-UT. (Fig. 2).

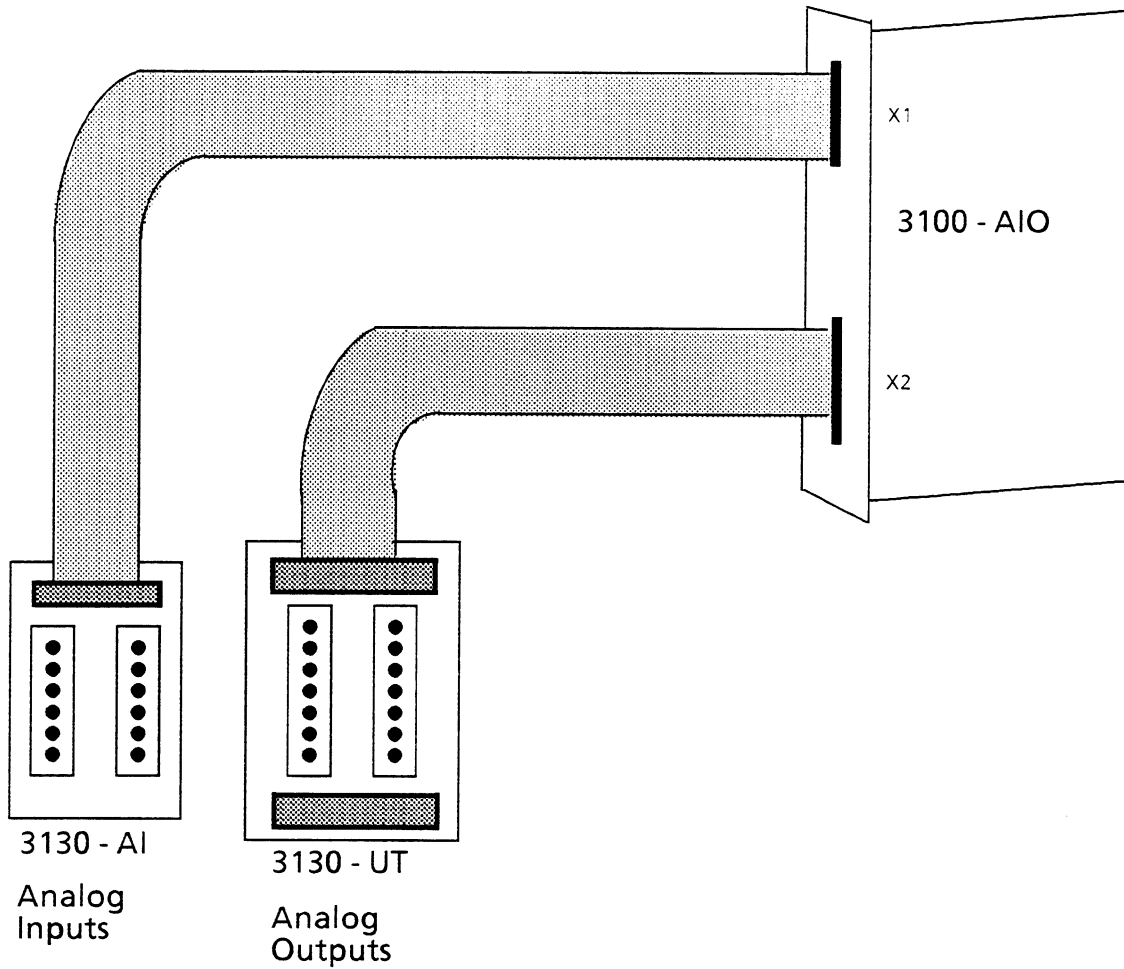


Figure 2. 3100-AIO Connection to Terminal Strips

Device Address

The base device address is selected by jumper array S1. 16 device addresses are reserved beginning at the base address. Valid base addresses are shown in Table 2.

Table 2. Base Address Selections

	S1	5-1	5-9	6-2	6-10	7-3	7-11	8-4	8-12
	LOGIC	1	0	1	0	1	0	1	0
BASE ADDRESS	10H		X		X		X	X	
	20H		X		X	X			X
	30H		X		X	X		X	
	40H		X	X			X		X
	50H		X	X			X	X	
	60H		X	X		X			X
	70H		X	X		X		X	
	80H	X				X		X	X
	90H	X				X		X	
	AOH	X				X			X
	BOH	X				X		X	
	COH	X			X			X	X
	DOH	X			X			X	X
	EOH	X			X		X		X

NOTE! Do not use device address OOH or FOH or a device address reserved for other boards in the rack.

The Assignment of Device Addresses Relative to the Base Address is shown in Table 3.

A 24V or 15V voltage can be connected to the board if one of the sensors requires such a supply voltage. Normally nothing is connected to connector X3. The voltage to be measured is connected to pins AIN (+) and AR (-). IT is the constant current (+) of the Pt-100 sensor and IR is its return line. (Fig. 3).

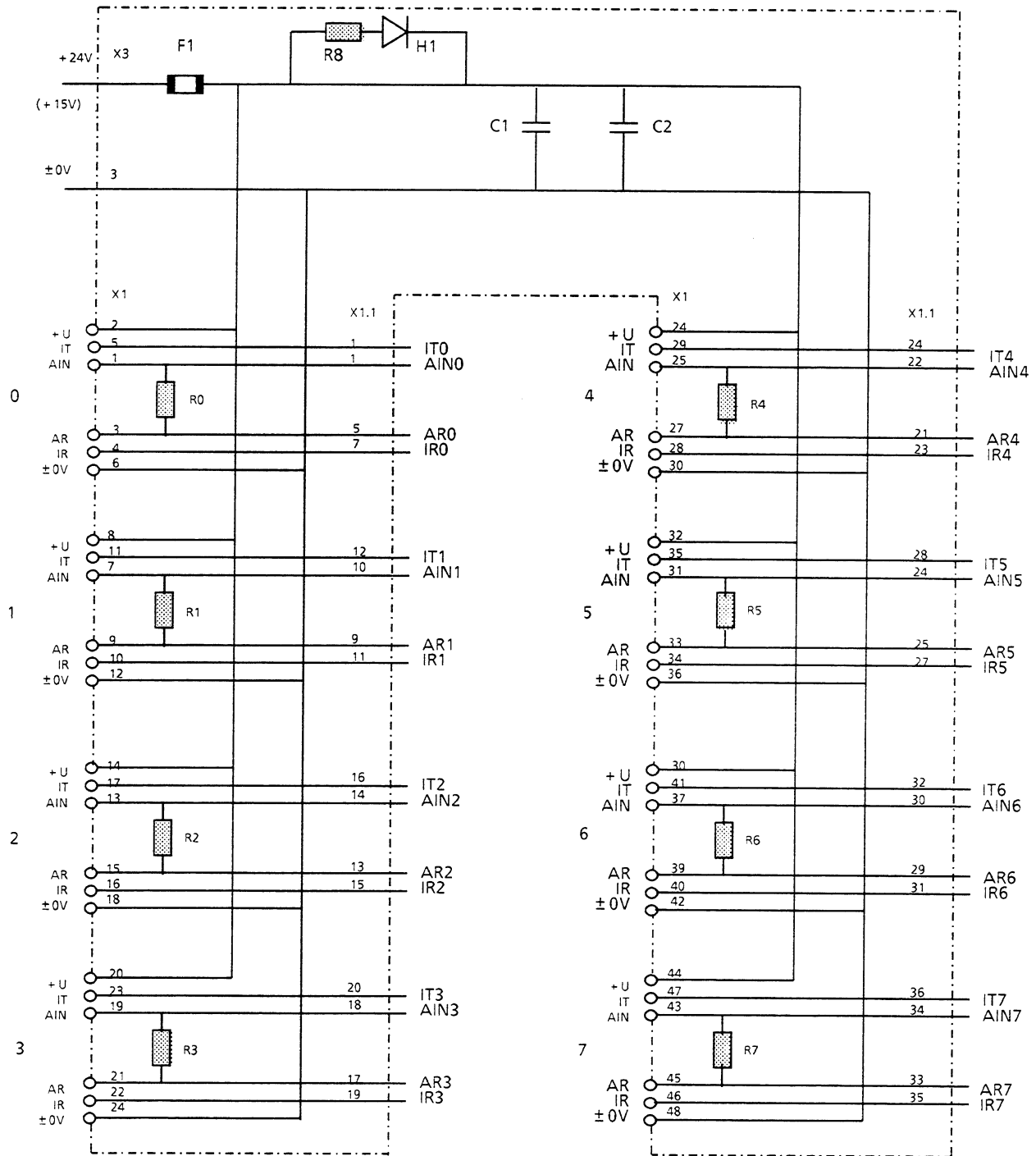


Figure 3. Terminal Strip Connection Diagram (Board 3130-AI)

Table 3. Device Address Assignments

OFFSET TO DEVICE ADDRESS	CHANNEL	TYPE CODE
0H	ANALOG INPUT 0	81H
1H	ANALOG INPUT 1	81H
2H	ANALOG INPUT 2	81H
3H	ANALOG INPUT 3	81H
4H	ANALOG INPUT 4	81H
5H	ANALOG INPUT 5	81H
6H	ANALOG INPUT 6	81H
7H	ANALOG INPUT 7	81H
8H	ANALOG OUTPUT 1	82H
9H	- NOT USED -	-
AH	ANALOG OUTPUT 2	82H
BH	- NOT USED -	-
CH	ANALOG OUTPUT 3	82H
DH	- NOT USED -	-
EH	ANALOG OUTPUT 4	82H
FH	- NOT USED -	-

The 3130-UT terminal strip board enables the analog outputs of two 3100-AIO boards to be connected to the process. 3130-UT has two connections like the example shown in Figure 4.

Normally nothing is connected to pins 1-4 and 37-40 of the terminal strips.

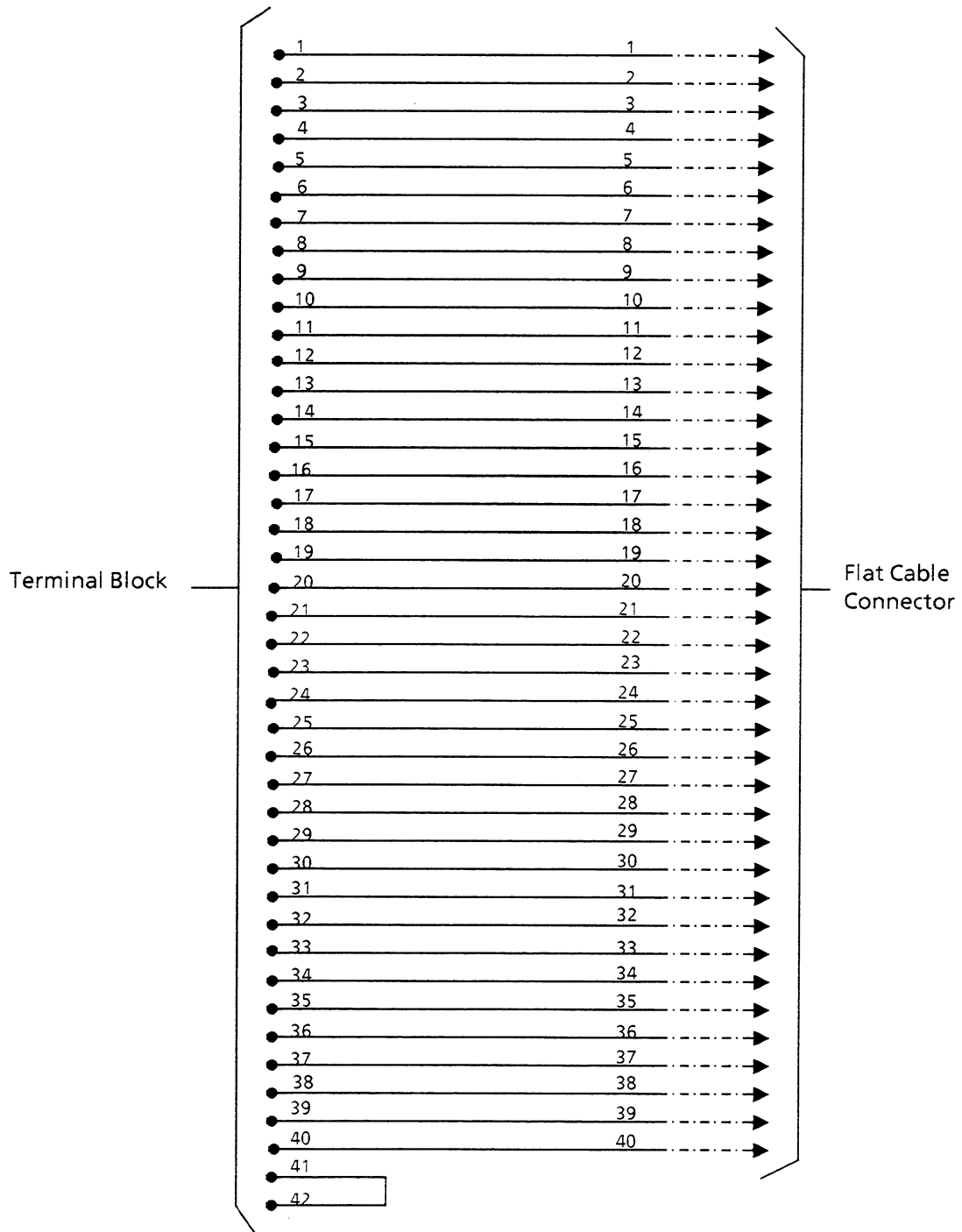


Figure 4. Terminal Strip Connections (3130-UT Board)

The signal list for the X2 connector of the 3100-AIO board and also for the terminal strip of the 3130-UT board is shown in Figure 5. Both the X2 connector and the 3130-UT terminal strip have the same numbering.

D/A Channel	Pin	Designation	Pin	Designation
	1	$\pm 0V$	21	NC
	2	$\pm 0V$	22	NC
	3	+ 15V	23	NC
	4	+ 15V	24	NC
0	5	UARO	25	NC
	6	AUO	26	NC
	7	IARO	27	NC
	8	IAO	28	NC
1	9	UARI	29	NC
	10	AUI	30	NC
	11	IAR1	31	NC
	12	IA1	32	NC
2	13	UAR2	33	NC
	14	UA2	34	NC
	15	IAR2	35	NC
	16	IA2	36	NC
3	17	UAR3	37	-15V
	18	UA3V	38	-15V
	19	IAR3	39	$\pm 0V$
	20	IA3	40	$\pm 0V$

NC = Not Connected

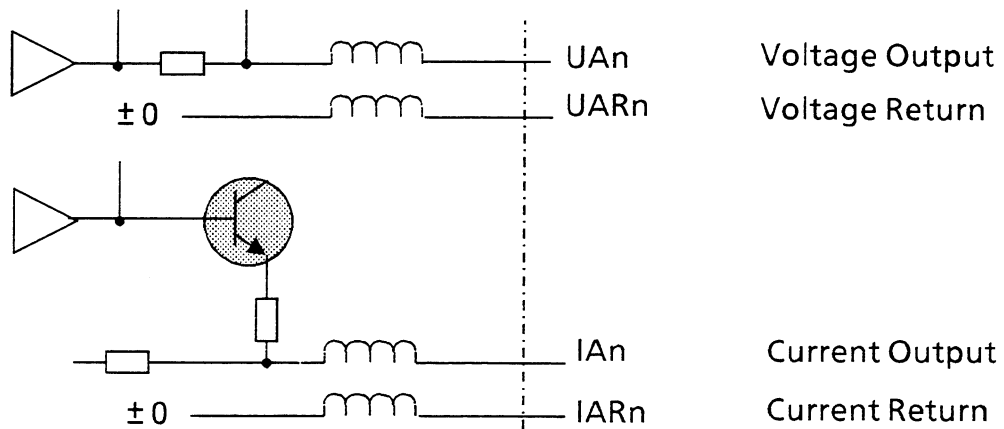


Figure 5. Input Signal List

The values of various input signals are shown in Figure 6. When making voltage or Pt-100 measurements, the shunt resistor must be removed.

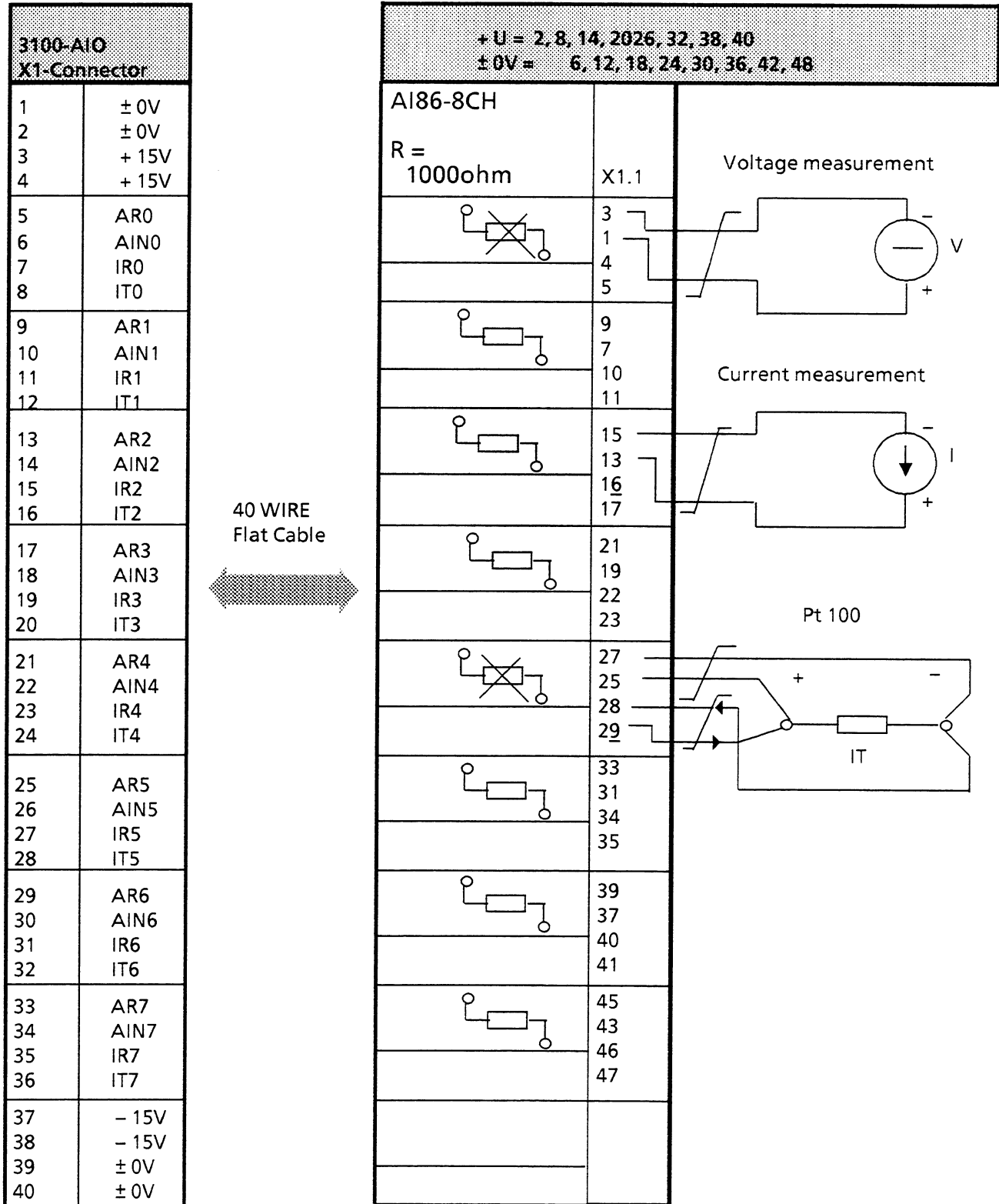


Figure 6. Input Signal Measurement