3100–CPU

DRC Central Processor PC Card Series A and B

General Description

The 3100–CPU Central Processor Unit Card contains both an Intel 8086 full 16–bit microprocessor and an 8087 floating point arithmetic processor. The combination of the coprocessor pair allows the card to process math functions using 32–bit floating point math, yielding numbers with 6 to 7 significant digits and exponents to 10 ± 38. The series A processor operates using a 5 MHz clock, while the series B processor utilizes an 8MHz clock.

In addition to the main coprocessor pair, the card contains circuitry to perform the following functions:

- Multi–task various function block programs at independent task intervals
- Operate command line interpreter to program function blocks
- Monitor and control DRC operation
- RS232 Communication interface for programming terminal connection
- Battery backed up clock calendar
- Bus driver circuitry to communicate to all other cards in rack
- Supervision of +5V DC supply voltage

Specifications

Power Requirements

5V DC @ 1.8 Amperes
+15V DC @ 0.02 Ampere
–15V DC @ 0.02 Ampere

Environment

Temperature: 0°C to 50°C (32°F to 120°F)
Relative Humidity: 5% to 95% non–condensing

Associated Function Blocks

DATE
SETDAT
IODINI
IINI
IWAIT

Description Of Operation

Several switches and jumpers located on the CPU card (Figure 1) are associated with the functions of the circuitry on the card. Some of the switches are integrally related with the internal configuration of the card and should never be changed from the initial setting listed in Table 1. Other switches may be changed depending on the specific type of application.

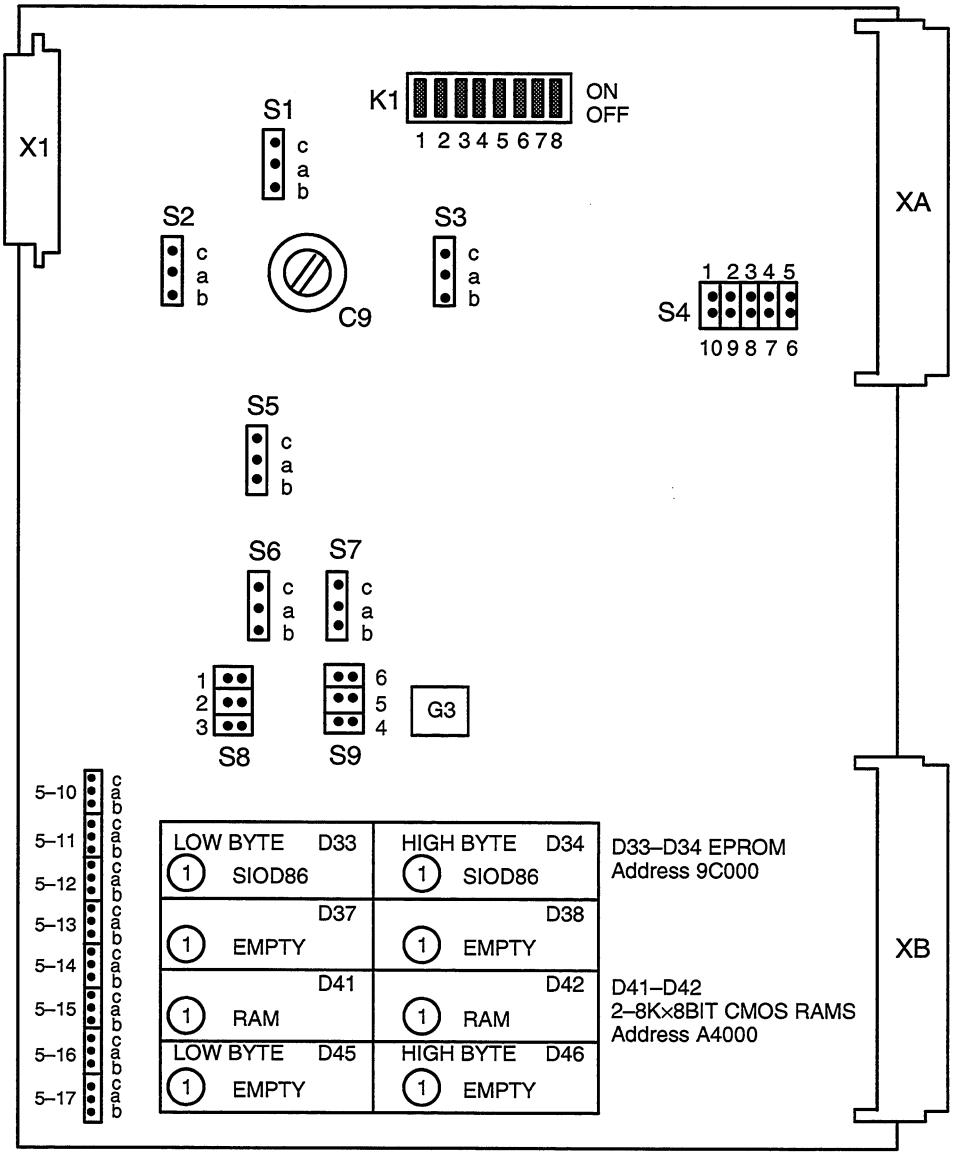

Figure 1. Component Layout

Table 1. CPU Jumper Position and Switch Settings

Switch	Position	Purpose
S1		Battery backup enable
	a–b*	Battery backup enabled (in use)
	a–c	Battery backup disabled
S2		Selection of low voltage signal for supply voltage supervision
	a–b*	Low voltage signal produced by CPU card. Board forms a power failure signal (PWF) to the bus (external power supply) from PCB Version F.
	a–c	Low voltage signal from backplane bus, pin A28c (coming from Rack Power Supply). Power failure signal (PWF) from the bus (all SEPUS).
	a–b–c	Board forms the power failure signal (PWF) to the bus (external power supply) from PCB Versions A–E.
S3		Selection of bus clock frequency (CMCLK)
	a–b	1.228800 MHz
	a–c*	2.457600 MHz
S4		Connection of internal interrupts
	1–10*	Receive from programming terminal RIR –> IR0 RXRDY
	2–9*	10ms task interrupt routine CIR –> IR1 TIMEF
	3–8	Power failure
	4–7*	Transmit to programming terminal TIR –> IR3 TXRDY
	5–6	8087 interrupt request
S5		Selection of **WAIT** cycles
	a–b	**WAIT** in all cycles
	a–c*	**WAIT** in I/O cycles only
S6		Selection of backup voltage for memory (D41 and D42)
	a–b	+5V DC rack supply
	a–c*	Voltage from CPU battery
S7		Selection of CPU clock frequency. (CPU base frequency f = crystal freq / 3)
	a–b	Clock frequency = f / 2
	a–c*	Clock frequency = f
S8		Memory **WAIT** time control
	1–6	2xCPU clock period
	2–5	3xCPU clock period
	3–4	4xCPU clock period
	5–6*	No **WAIT** period
S9		I/O **WAIT** time period (Extensions of I/O cycles)
	1–6	2xCPU clock period
	2–5	3xCPU clock period
	3–4*	4xCPU clock period
	5–6	No **WAIT** period
S10 through S17		Memory type selection
	a–b	2k × 8 bits
	a–c*	8k × 8 bits
K1		Selects Baud rates for communication to programming terminal. Refer to Table 2 for detailed switch settings.
C9	VARJ	Real time clock oscillator frequency adjustments.
G3	15.000 MHz 24.000 MHz	Processor crystal with frequency marked.

* Indicates normal jumper position.

Memory

Eight memory chip sockets located in the lower left corner of the CPU Card may be used to hold EPROM and RAM chips with a total capacity of 64k bytes maximum, of which 16k byte can be battery backed up. In all systems, positions D33 and D34 are used for the EPROM chips which contain the firmware required to drive the communication interface between the CPU card and the programming terminal. Positions D41 and D42 are used for two 8k, 8–bit RAM chips. Information stored in the RAM memory on the CPU consists of the information for the clock calendar, memory pointers to the main system memory, interrupt control vectors, and other information.

Battery Back Up

Information stored in the RAM memory in chip positions D41 and D42 can be battery backed up when control power is discontinued. Jumper switch S6 determines which power supply is used to power the RAM memory.

In addition to the back up of the RAM memory, the battery is used to maintain the operation of the real time clock calendar circuit in the event of a power loss in the rack. Use of the battery back up may be disabled by jumper switch Sl.

IMPORTANT: Battery backup of the RAM, memory requires that Sl be in the a–b position and S6 be in the a–c position.

Supply Voltage Supervision

The CPU card contains on–board circuitry which monitors the +5V DC logic supply voltage. If the voltage drops to +4.6V DC, the CPU card produces a low voltage signal which is used to inhibit operation of the clock calendar circuit and the RAM memory from the normal rack power supply. In this case, the battery backup is used to provide power for these functions. Once the low voltage signal has been tripped, the inhibit command will not be removed until the voltage again rises to +4.7V DC.

Supervision of the +5V DC power supply may also be performed in the rack power supply.

IMPORTANT: If an undervoltage condition is detected, the card will maintain the clock calendar and RAM memory only if switches Sl and S6 are in proper positions.

Interrupt Control

Circuitry for a programmable interrupt circuit is located internal to the CPU Card and allows for real time interrupt routing to be implemented in the CPU. Several of the interrupt routines are a fixed part of the normal operation of the CPU and therefore must not be changed.

Five of the interrupt functions are enabled through jumper switch positions on S4. Refer to Table 1 for a definition of the switch positions and positions required for normal system operation. Three other switches (S5, S8 and S9 are associated with the configuration of the **WAIT** cycle routine associated with the interrupt function and will always be set as shown in Table 1.

Interrupts 5, 6 and 7 can be event driven by a special input board (DI86–M8/8) and programmed using the IINI and IWAIT function block.

Communication Interface

The CPU Card contains all hardware required for the interface between the DRC and the programming terminal. Communication is provided through the use of a programmable communication controller and a UART communication chip which provides one full duplex RS–232 communication link. The baud rate for communication to the programming terminal is determined by positions on switch Kl (Table 2).

Table 2. Selection of Baud Rate

	K1							
Baud Rate	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**
50	X	X	0	1	0	0	X	X
75	X	X	1	1	0	0	X	X
110	X	X	1	1	1	1	X	X
134.5	X	X	0	0	1	0	X	X
200	X	X	1	0	1	0	X	X
300	X	X	1	0	1	1	X	X
600	X	X	0	1	1	0	X	X
1200	X	X	1	1	0	1	X	X
1800	X	X	0	1	0	1	X	X
2400	X	X	0	0	1	1	X	X
4800	X	X	1	0	0	1	X	X
9600	X	X	0	0	0	1	X	X
19200	X	X	1	0	0	0	X	X
19200	X	X	0	0	0	0	X	X

Logic 1 = Switch OPEN
Logic 0 = Switch ON
X = Don't Care

The default character structure for the terminal is:

- 7 data bits
- Even parity
- 2 stop bits

The CPU card can examine the character structure of the terminal and configure itself to match when the "CONTROL" and "B" keys are simultaneously pressed followed by several keys pressed in numerical order (i.e. 1, 2, 3).

Although it is possible for the programming terminal to be connected directly to the Xl connector of the CPU card, it is recommended that connection to the programming terminal be made through the Program, Test, Run switch (3110–MSC) hardware mounted separately (Figure 2). This allows for control of the operational mode of the programming terminal using the switch and reduces the possibility of signal noise entering the CPU through the Xl connector.

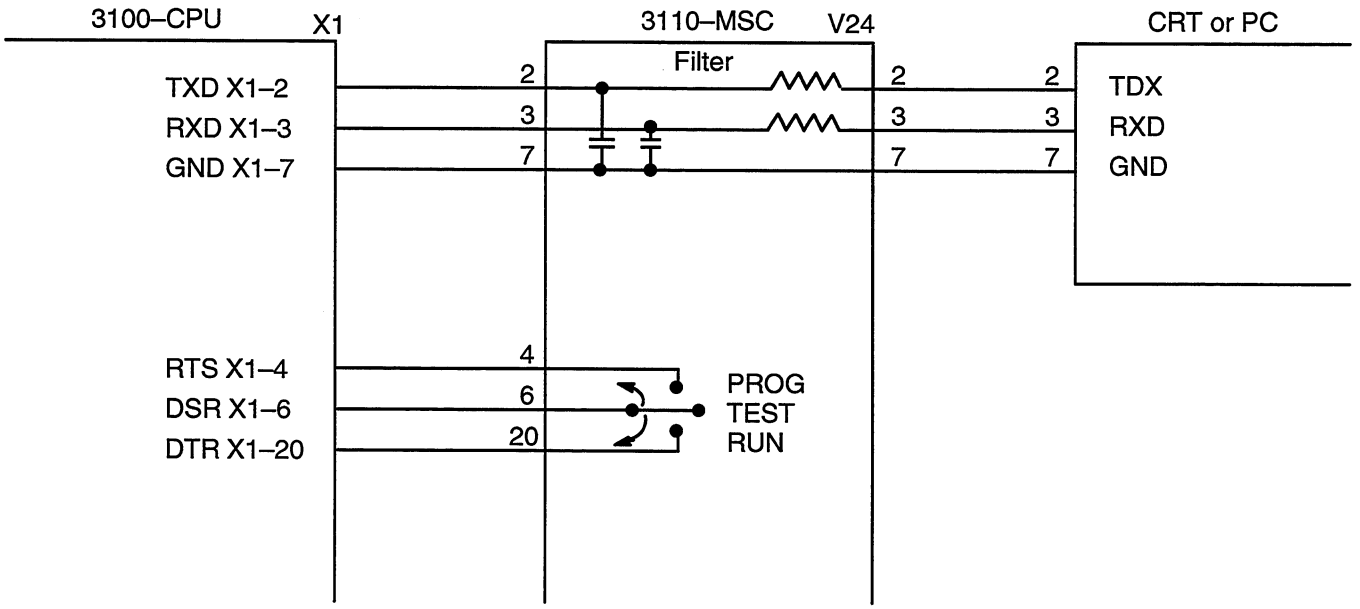

Figure 2. Connection of Programming Terminal

Date Setting

The date setting normally performed in a system program using a SETDAT Block may also be performed directly from the DRC Programming Terminal. To set the date, the DRC must be in the Program or Test Mode and the system prompt (*) must appear on the screen. Option 9 of the Help function allows you to read the present date and time and to enter a new date and time. For further information on use of the Help command, refer to the DRC Terminal Operation Manual.

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