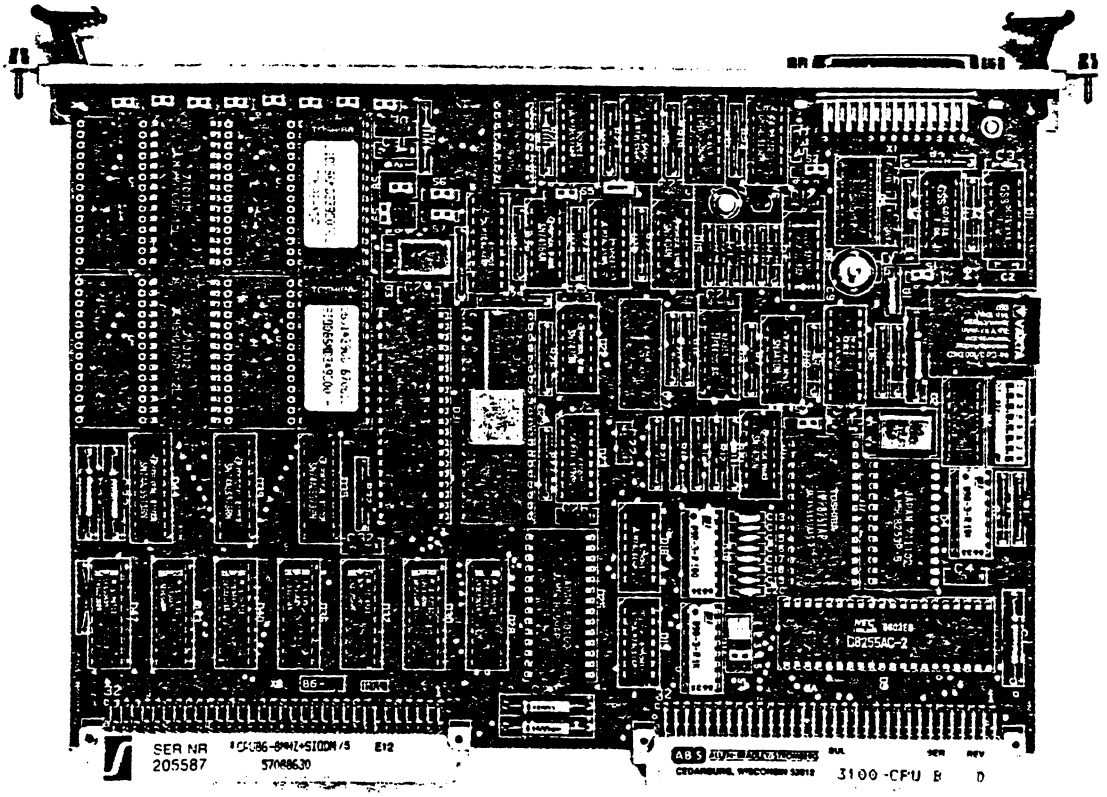
Bulletin 3100-CPU

DRC Central Processor PC Card Series A and B



3100-CPU

Description

The 3100-CPU Central Processor Unit Card contains both an Intel 8086 full 16-bit microprocessor and an 8087 floating point arithmetic processor. The combination of the 8086/8087 co-processor pair allows the CPU Card to process math functions using 32 bit floating point math, yielding numbers with 6 to 7 significant digits and exponents to 10 ±38. The series A processor operates using a 5 MHz clock, while the series B processor utilizes an 8 MHz clock. -

In addition to the main coprocessor pair, the CPU Card contains circuitry to perform the following functions:

- chip plugs for up to 64k-bytes of memory. Of this, 16k bytes can be battery backed up.
- programmable interrupt controller
- programmable interval timer
- programmable communication interface
- programmable peripheral interface
- battery backed up clock calendar
- bus driver circuitry
- supervision of +5V DC supply voltage

Specifications

Location	CPU Rack
Power Requirements	5V DC @1.8 Amperes +15V DC @0.02 Ampere −15V DC @0.02 Ampere
Environment	**Temperature:** 0° C to 50° C (32° F to 120° F) **Relative Humidity:** 5% to 95% non-condensing

Associated Functional Blocks

DATE, SETDAT, IODINI, IINI, IWAIT

Description of Operation

Several switches and jumpers located on the CPU card are associated with the functions of the circuitry on the card. Some of the switches are integrally related with the internal configuration of the card and should never be changed from the initial settings listed in Table 1. Other switches may be changed depending on the specific type of application.

Memory

Eight memory chip sockets located in the lower left corner of the CPU Card (Figure 2) may be used to hold EPROM and RAM chips with a total capacity of 64k bytes maximum, of which 16k bytes can be battery backed up. In all systems, positions D33 and D34 are used for the EPROM chips which contain the firmware required to drive the communication interface between the CPU card and the programming terminal. Positions D41 and D42 are used for two 8k, 8-bit RAM chips. Information stored in the RAM memory on the CPU consists of the information for the clock calendar, memory pointers to the main system memory, interrupt control vectors,and other information. Positions D37, D38, D45 and D46 are not used. Several jumpers located to the left of the memory chips are used to indicate to the processor the portion of memory that is to be battery backed up. For all applications, switches S10 thru S17 must be in the **a-c** position.

Battery Back Up

Information stored in the RAM memory in chip positions D41 and D42 can be battery backed up when control power is discontinued. Jumper switch S6 determines which power supply is used to power the RAM memory. When switch S6 is in the **a-b** position, the RAM is powered by the external +5V DC supply from the backplane. In this case, when power to the rack is lost, the information in the RAM will also be lost. When S6 is in the **a-c** position, information in the RAM memory will be maintained thru use of the CPU on-board battery if rack power is lost. For normal operation,S6 is in the **a-c** position.

In addition to the back up of the RAM memory, the battery is used to maintain the operation of the real time clock calendar circuit in the event of a power loss in the rack. Use of the battery back up may be disabled by jumper switch S1. If the CPU card is to be stored for long periods of time without external power, and it is not necessary to maintain the clock calendar and RAM memory, switch S1 may be placed in the **a-c** position which disconnects the battery from the CPU circuitry to prolong battery life. During normal operation in a rack, S1 must be in the **a-b** position, enabling use of the battery.

IMPORTANT: Battery back up of the RAM memory requires that S1 be in the **a-b** position and S6 be in the **a-c** position.

Supply Voltage Supervision

The CPU card contains on-board circuity which monitors the +5V DC logic supply voltage. If the voltage drops to +4.6V DC, the CPU card produces a low voltage signal which is used to inhibit operation of the clock calendar circuit and the RAM memory from the normal rack power supply. In this case, the battery back-up is used to provide power for these functions. Once the low voltage signal has been tripped, the inhibit command will not be removed until the voltage again rises to +4.7V DC.

Supervision of the +5V DC power supply may also be performed in the rack power supply. In this case, the power supply provides the low voltage signal to the CPU card thru one of the pins connected to the backplane bus. The low voltage signal can only originate from one source. Switch S2 determines the device used to provide the low voltage signal. With S2 in the **a-b** position, supervision is by the CPU card; however, with S2 in the **a-c** position, the low voltage signal is provided by the rack power supply. Under normal operation, the supply voltage supervision is provided in the power supply (S2 in the **a-c** position).

IMPORTANT: If an undervoltage condition is detected, the card will maintain the clock calendar and RAM memory only if switches S1 and S6 are in proper positions.

Interrupt Control

Circuitry for a programmable interrupt circuit is located internal to the CPU Card and allows for real time interrupt routines to be implemented in the CPU. Several of the interrupt routines are a fixed part of the normal operation of the CPU and therefore must not be changed. The interrupts are defined as follows:

- Interrupt 0 occurs whenever the CPU communication hardware receives an incoming message from the the programming terminal.
- Interrupt 1 occurs every 10ms and is the basic task timing interrupt routine.
- Interrupt 2 occurs only when a power failure occurs.
- Interrupt 3 occurs whenever the CPU communication hardware transmits an outgoing message to the programming terminal.
- Interrupt 4 is reserved for the disk controller and is controlled by several function blocks associated with the disk control function (**DSKCLO, DSKOPE, DSKRD and DSKWR**).
- Interrupt 5 is a programmable interrupt which is controlled by use of interrupt function blocks **IINI** and **IWAIT**.
- Interrupt 6 is reserved for use by the 8087 coprocessor or is a programmable interrupt which is controlled by use of interrupt function blocks **IINI** and **IWAIT**.
- Interrupt 7 is a programmable interrupt which is controlled by the use of interrupt function blocks **IINI** and **IWAIT**.

Five of the interrupt functions are enabled through jumper switch positions on S4. Refer to Table 1 for a definition of the switch positions and positions required for normal system operation. Three other switches (S5, S8 and S9) are associated with the configuration of the **WAIT** cycle routine associated with the interrupt function and will always be set as shown in Table 1.

Communication Interface

The CPU Card contains all hardware required for the interface between the DRC and the programming terminal. Communication is provided through the use of a programmable communication controller and a USART communication chip which provides one full duplex RS-232 communication link. Connector X1 on the CPU Card provides for connection to the programming terminal through the use of a 25 pin, D type connector. Wiring to connector X1 uses standard CRT line numbers as shown in Figure 1. The baud rate for communication to the programming terminal is determined by positions on switch K1 (Table 2).

Although it is possible for the programming terminal to be connected directly to the X1 connector of the CPU card, it is recommended that connection to the programming terminal be made through the Program, Test, Run switch (3130-MSC) hardware mounted on the CPU rack power supply. This allows for control of the operational mode of the programming terminal using the switch and reduces the possibility of signal noise entering the CPU through the X1 connector.

Date Setting

The date setting normally performed in a system program using a SETDAT Block may also be performed directly from the DRC Programming Terminal. To set the date, the DRC must be in the Program or Test Mode and the system prompt (*) must appear on the screen. Option 9 of the Help function allows you to read the present date and time and to enter a new date and time. For further information on use of the Help command, refer to the DRC Terminal Operation Manual.

Table1. CPU Jumper Position And Switch Settings

SWITCH	POSITION	PURPOSE
S1		Battery back up enable
	a-b*	Battery back up enabled
	a-c	Battery back up disabled
S2		Selection of low voltage signal for battery control of the clock calender
	a-b	Low voltage signal produced by CPU card
	a-c*	Low voltage signal from backplane bus, pin A28c (coming from Rack Power Supply)
S3		Selection of bus clock frequency
	a-b	1.228800 MHz
	a-c*	2.457600 MHz
S4		Connection of internal interrupts
	1-10*	Receive from programming terminal
	2-9*	10ms task interrupt routine
	3-8	Power failure
	4-7*	Transmit to programming terminal
	5-6	8087 interrupt request
S5		Selection of **WAIT** cycles
	a-b	**WAIT** in all cycles
	a-c*	**WAIT** in I/O cycles only
S6		Selection of back up voltage for memory
	a-b	+ 5V DC Rack supply
	a-c*	Voltage from CPU battery
S7		Selection of CPU clock frequency. (CPU base frequency f = crystal freq ÷ 3)
	a-b	Clock frequency = f ÷ 2
	a-c*	Clock frequency = f
S8		Memory **WAIT** time control
	1-6	2xCPU clock period
	2-5	3xCPU clock period
	3-4	4xCPU clock period
	5-6*	No **WAIT** period
S9		I/O **WAIT** time period
	1-6	2xCPU clock period
	2-5	3xCPU clock period
	3-4*	4xCPU clock period
	5-6	No **WAIT** period
S10		Memory type selection
thru	a-b	2k x 8 bits
S17	a-c*	8k x 8 bits
K1		Selects Baud rates for communication to programming terminal Refer to Table 2 for detailed switch settings.

* Indicates normal jumper position

Table 2. Selection Of Baud Rate

Baud Rate	K1							
	S1	S2	S3	S4	S5	S6	S7	S8
50	X	X	1	0	1	1	X	X
75	X	X	0	0	1	1	X	X
110	X	X	0	0	0	0	X	X
134.5	X	X	1	1	0	1	X	X
200	X	X	0	1	0	1	X	X
300	X	X	0	1	0	0	X	X
600	X	X	1	0	0	1	X	X
1200	X	X	0	0	1	0	X	X
1800	X	X	1	0	1	0	X	X
2400	X	X	1	1	0	0	X	X
4800	X	X	0	1	1	0	X	X
9600	X	X	1	1	1	0	X	X
19200	X	X	0	1	1	1	X	X
19200	X	X	1	1	1	1	X	X

Logic 1 = Switch ON
Logic 0 = Switch OFF
X = Don't Care

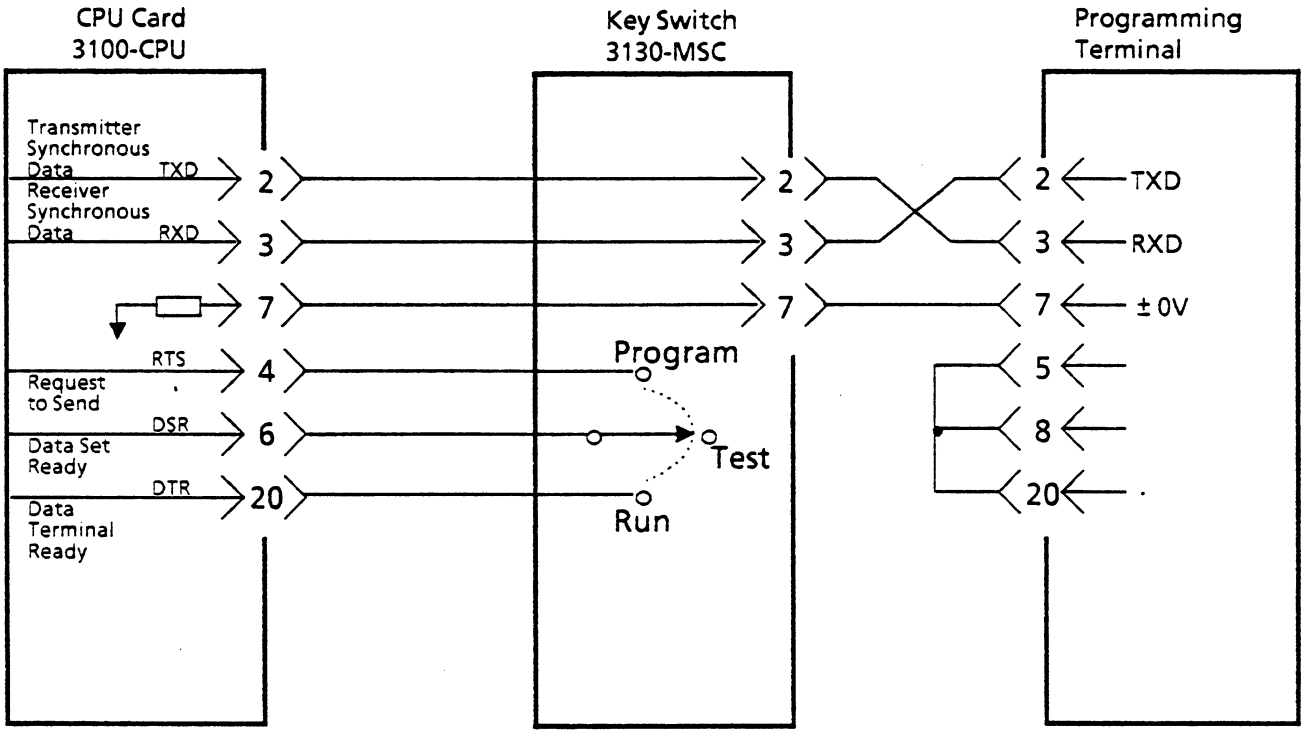


Figure 1. Connections To Programning Terminal

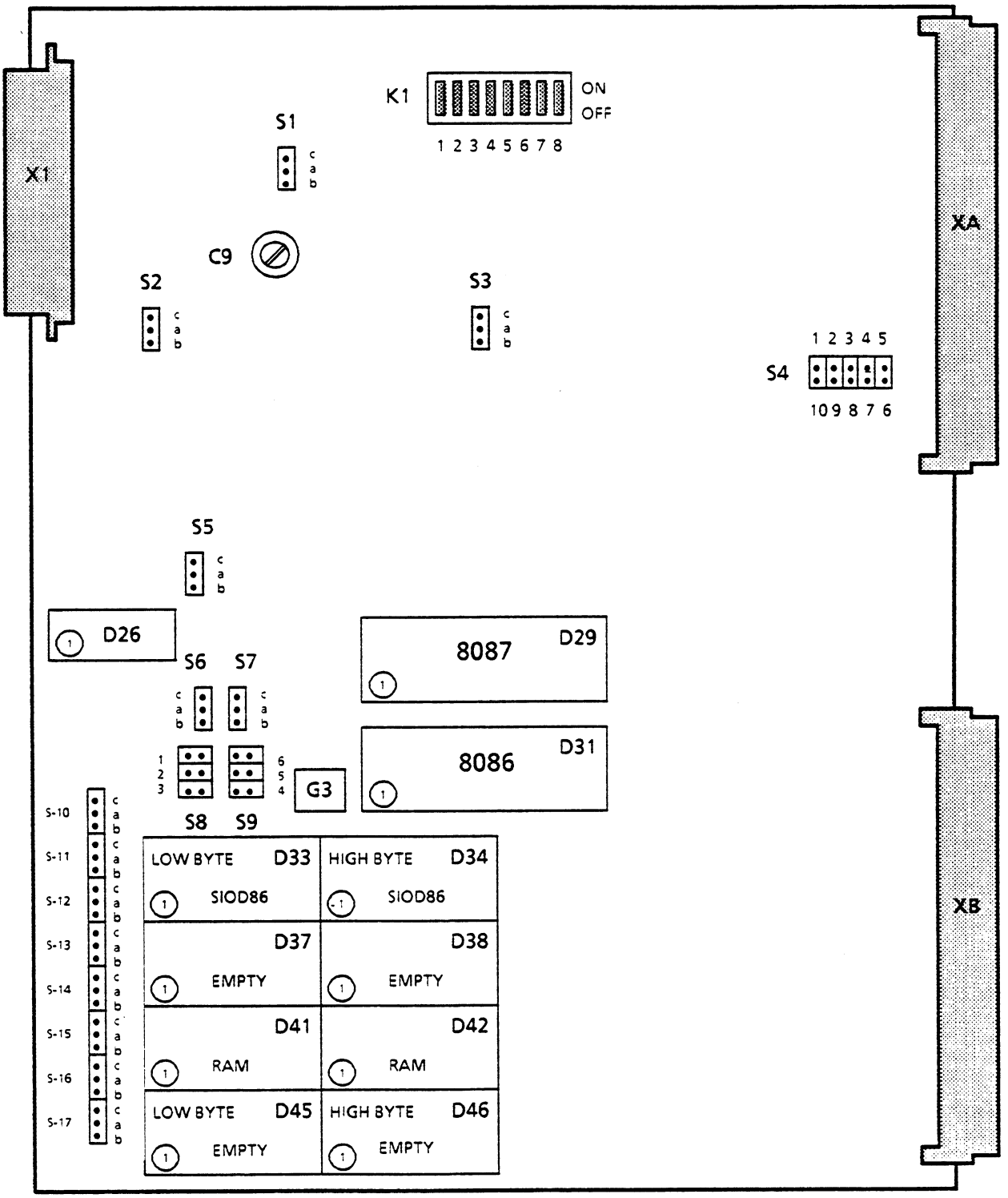


Figure 2. Location Of Jumpers And Switches On The 3100-CPU Card