Bulletin 3100-I01

DRC I/O Processor PC Card Series A&B

PHOTO REQUIRED

3100-IO1 Series A

General Description

The 3100-I01 I/O (Input/Output) Processor Card contains, among other hardware, an intel 8086 full 16-bit microprocessor and an 8087 floating point arithmetic processor. The card allows for the addition of one DRC I/O rack per card. A maximum of 4 I/O Processor cards may be used in a single DRC. The purpose of the I/O Processor card is to process the flow of data between the main CPU located on the CPU Card and I/O cards located on a separate I/O rack.

In addition to the main co-processor pair, there is hardware on the I/O Processor Card used to perform the following functions:

- chip plugs for up to 32 K-bytes of memory
- Programmable interrupt controller
- Programmable interval timer
- bus driver circuitry

Specifications

Location	CPU Rack
Power Requirements	5V DC@ 2.8 Ampere
Environment	**Temperature:** 5° C to 50° C (40° F to 120° F) **Relative Humidity:** 5% to 95% non-condensing

Indicators

IOD LED - board has memory control
IO LED - ref to I/O rack
BHLDA LED - CPU has memory
HOLD LED - CPU req. memory control
SRES LED - Static reset

Selections

IOD board memory address (S2-5)
IO Operations set-up (S1)

Associated Functional Blocks

IODINI, IODIAG

Description of Operation

The I/O Processor Card allows for the addition of one I/O rack per card (Figure 1). Switch settings on the card determine the memory address of the I/O Processor Card and correspond to the I/O rack number. A maximum of 4 I/O Processor Cards may be used. The main CPU rack, which contains the CPU Card is always designated Rack 0. I/O racks are then numbered 1thru 4 sequentially starting at 1 for the first rack, etc. I/O rack numbers cannot be skipped, therefore, if there is only one I/O rack, it must be Rack 1, if there are two racks, they must be Rack 1 and 2, etc.

The I/O Processor Card contains memory which is used as shared memory by the CPU Card, therefore, the I/O Processor Card must be located in the CPU rack. In addition to the I/O Processor Card located in the CPU rack, an I/O Transceiver Card (3100-I02) must be located in the I/O rack. A 40 pin ribbon cable transfers data between the I/O Processor card and the I/O Tranceiver Card. The I/O Tranceiver Card controls the flow of data between I/O Cards located on the I/O rack, and the I/O Processor Card. Refer to the I/O Tranceiver Card Component Description for a description of that card.

Memory

On the card, there are 4 memory chip sockets located in the lower right corner (Figure 1), which contain 32 K-bytes of RAM memory which is used as shared memory by both the I/O Processor card and the CPU Card. In addition to the 32 K of RAM memory, the programmable interrupt controller and programmable interval timer are assigned an additional 32K of memory addresses by the CPU Card. This means that the I/O Processor Card reserves a total of 64 K-bytes in the CPU memory map.

The memory address used by the CPU Card is a 5 digit hexadecimal number. The first four digits specify memory addresses as shown in Figure 3. The most significant digit determines the memory allocation of the shared memory from the point of view of the CPU Card. The starting address of the 64 K-bytes of memory assigned to the I/O Processor Card is determined by the switch settings of S2-S5. Each switch is a jumper where position **a-b** represents logic 1 and position **a-c** represents logic 0. The address assigned to the I/O Processor Card corresponds to the card number, and therefore I/O rack number as shown in Table 1.

Table 1. I/O Processor Card Number Setting

S2	S3	S4	S5	Memory Area	Card (Rack) Number
a-b	a-c	a-b	a-c	A0000-AFFFF	0*
a-b	a-c	a-b	a-b	B0000-BFFFF	1
a-b	a-b	a-c	a-c	C0000-CFFFF	2
a-b	a-b	a-c	a-b	D0000-DFFFF	3
a-b	a-b	a-b	a-c	E0000-EFFFF	4

* indicates normal jumper position

Interrupt and Wait Control

The RAM memory on the card is accessed by both the CPU Card and the 8086 processor on the I/O Processor. In order to control data flow, a programmable interrupt controller determines which processor has access to the data in the RAM memory. The card has been set so that access of memory by the CPU processor takes precedence over the processor located on the I/O Processor Card. When the CPU processor is accessing memory, the processor on the I/O Processor Card is put into a WAIT state until the CPU Card is finished. In order for the processor on the I/O Processor Card to access data if an interrupt from the CPU Card occurs, the read and write times are extended. Switch S1 determines the time extension for reading and writing. Switch positions are defined in Table 2.

Table 2. S1 Switch Settings

Position	Read Time (ns)	Write Time (ns)
1 - 8	1400	1200
2 - 7	1600	1400
3 - 6*	1800	1600
2 - 5	2000	1800

* indicates normal jumper position

Data Transfer

Data transfer between the I/O Processor Card and the I/O cards located in the I/O rack is controlled by the I/O Tranceiver Card located in the I/O rack. Figure 6 illustrates the circuitry associated with the transfer of data. Refer to the I/O Tranceiver Component Description for a detailed description of the I/O Tranceiver Card.

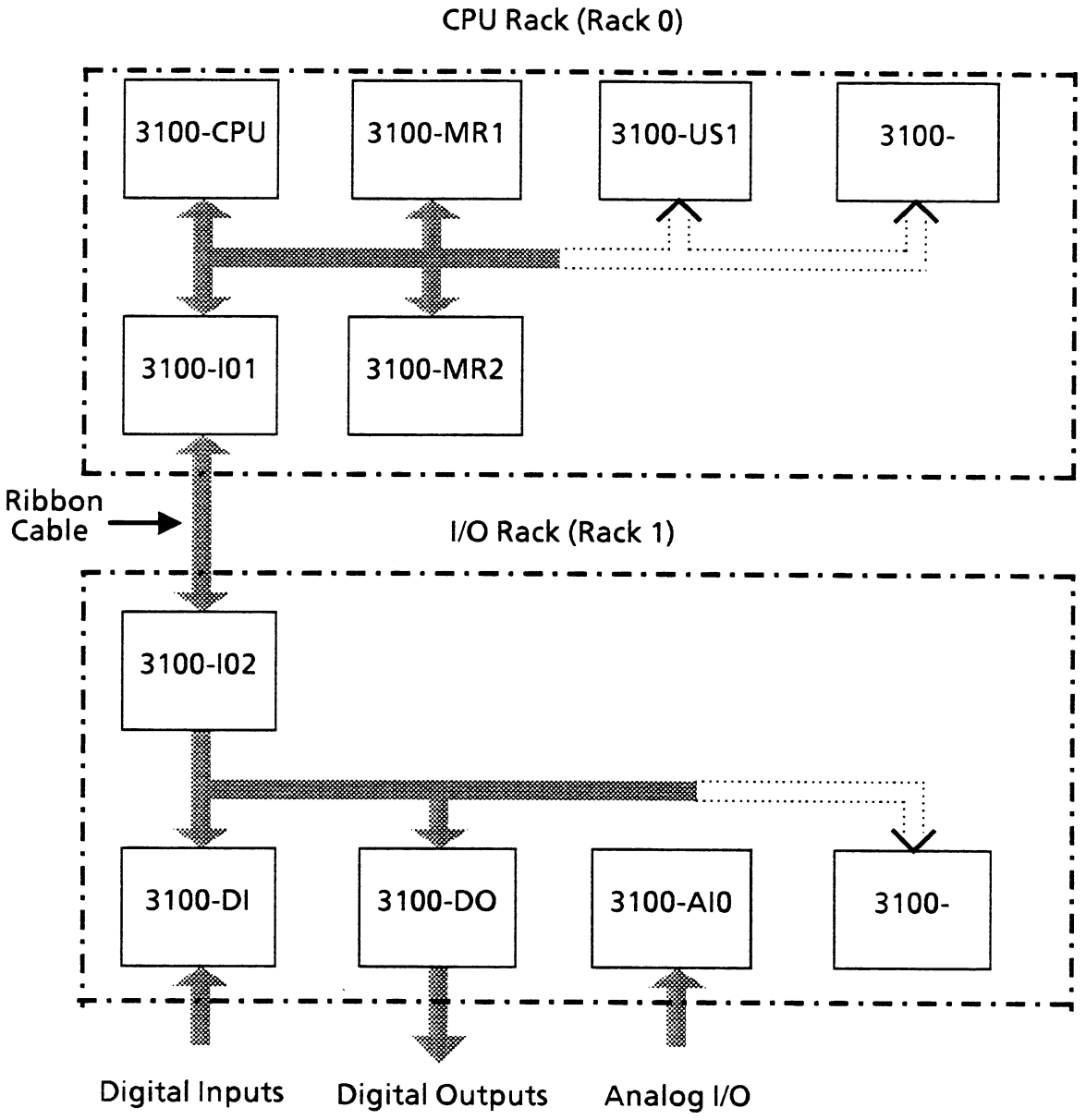

Figure 1. I/O Processor Card used for the addition of 1 I/O Rack

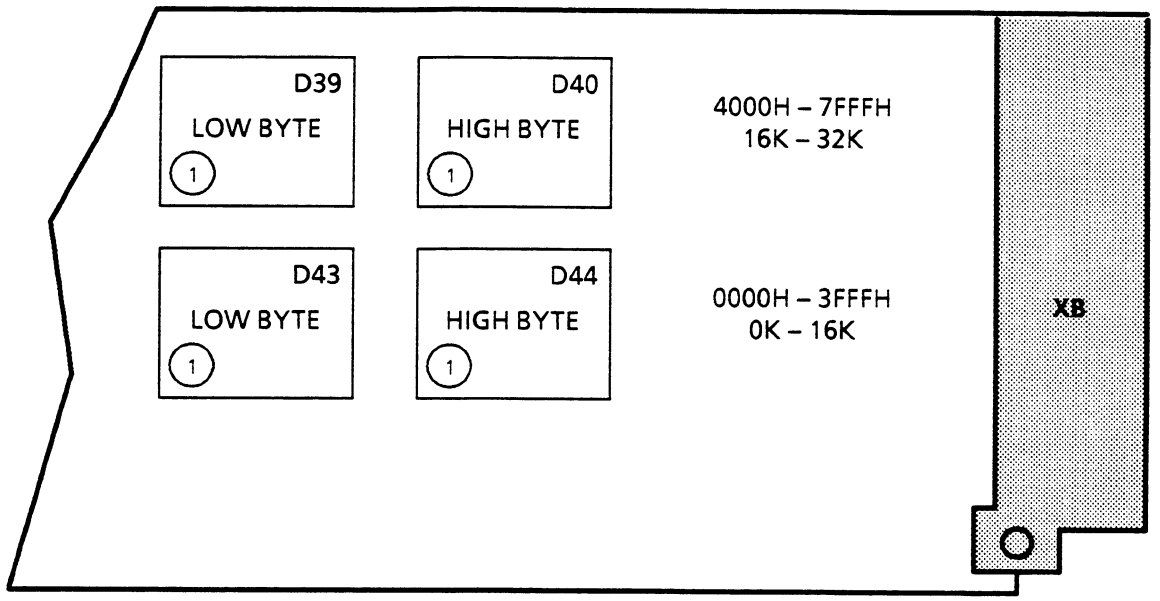

Figure 2. Memory Circuit Location

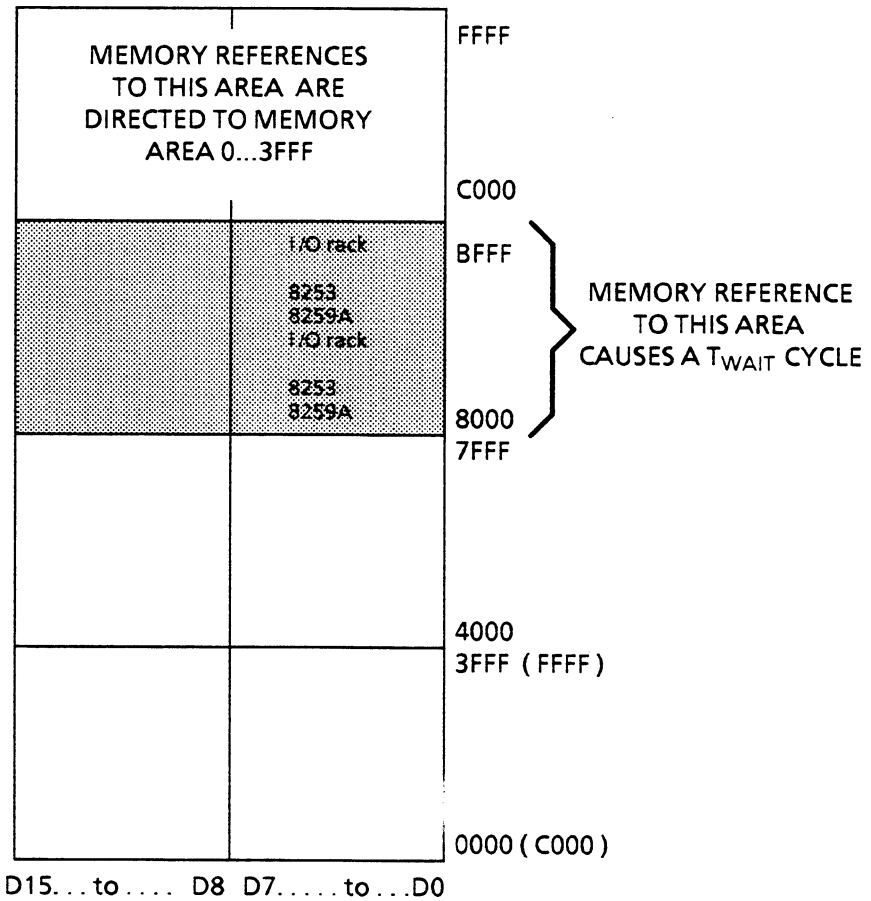

Figure 3. Memory Space Allocation

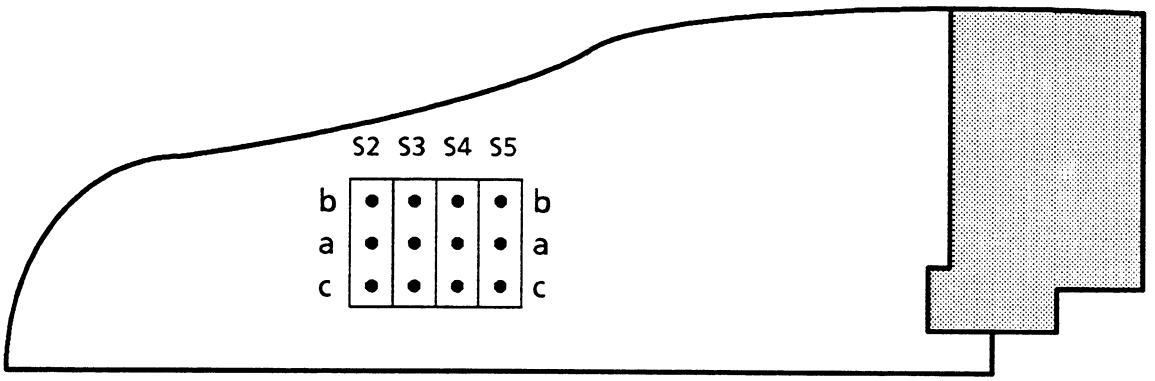

Figure 4. Location of Address Selection Jumpers on Lower Edge of Card

Status Indicators

When illuminated, the five Light Emitting Diodes (LEDs) located on the 3100-IO1 Card (Figure 5) indicate the following:

IOD: The board memory is available to 3100-IO1

IO: Memory references have been made to the IO rack.

BHLDA: Memory of the 3100-IO1 Card is available to the 3100-CPU Card. This can result from one of the following:

- 3100-CPU Card has taken possession of the 3100-IO1 Card memory
- the HOLD signal is in "1" state
- the SRES signal is in "1" state
- 3100-CPU Card memory access to memory space of 3100-IO1 Card

HOLD: A request to use the 3100-IO1 Card memory (the 3100-CPU Card has referenced the given memory or SHOLD is in the "1" state).

SRES: SRES or the programmable RESET given by the 3100-CPU Card is valid. The 8086 of the 3100-IO1 Card is in the "RESET" state and the memory of 3100-IO1 Card is available to the 3100-CPU Card.

Refer to Table 3 for a description of control signals.

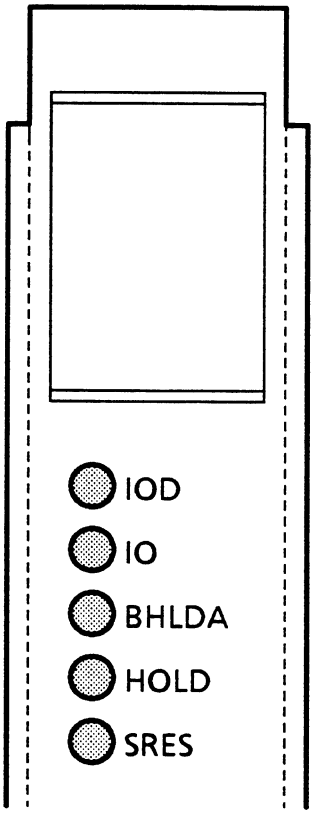

Figure 5. Location of LEDs

Table 3. Control Signals

Designation	In/Out	Meaning
SHOLD	IN	Override signal from the 3100-CPU Card; when in the "1" state, 3100-IO1 Card is in the WAIT state and its memory is available to the CPU.
SRES	IN	Overriding signal from the 3100-CPU Card; when it is in the "1" state, the 8086 of 3100-IO1 Card is in the RESET state and memory is available to the 3100-CPU Card, the I/O rack being in RESET state.
$\overline{\text{NMI}}$	IN	Non-maskable Interrupt input to the 8086 of the 3100-IO1 Card.
HOLD	IN	Memory access request from 3100-CPU Card

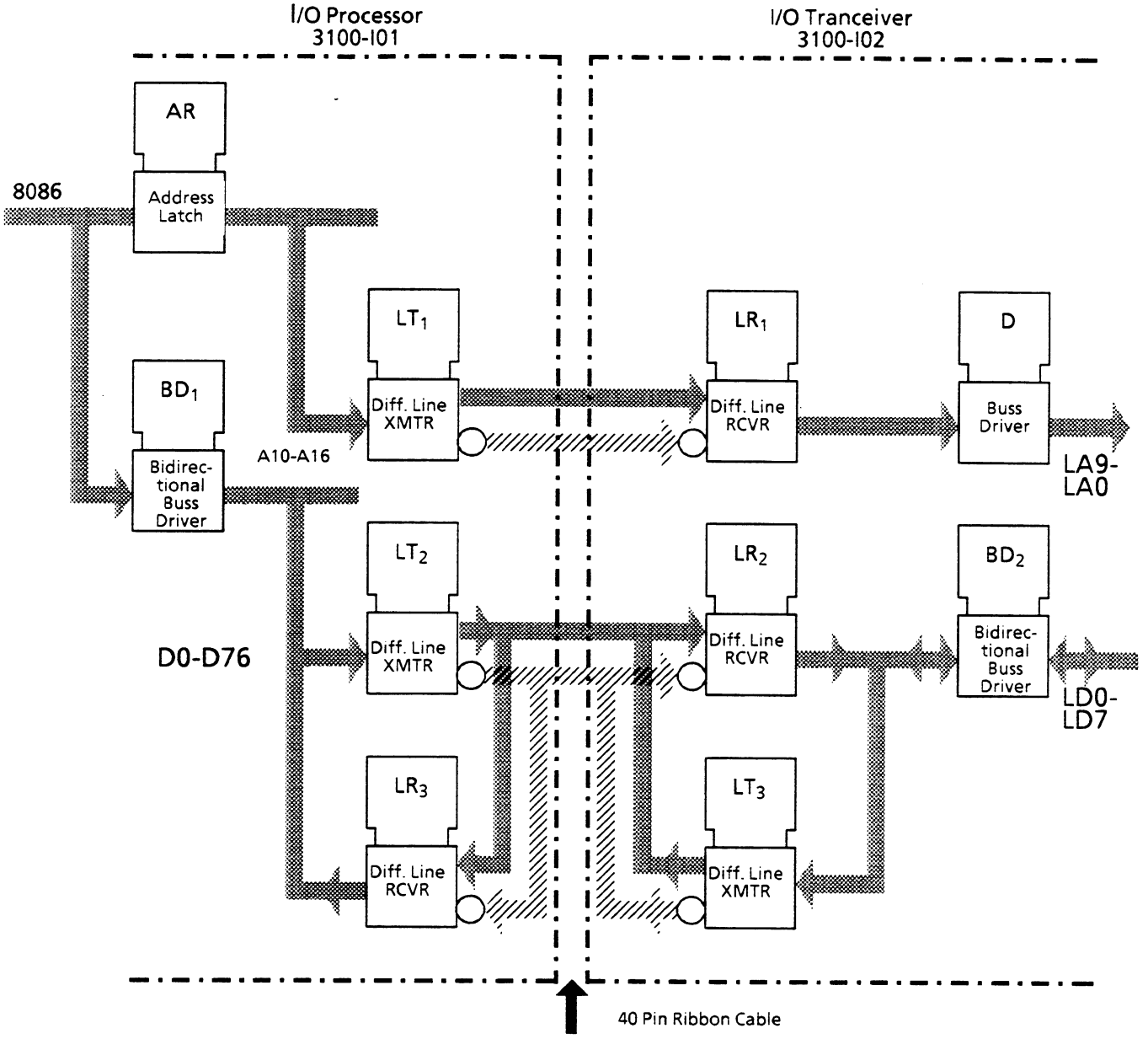

Figure 6. Data Transfer between I/O Processor and I/O Tranceiver Cards

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