3100–MEM

MEM86–3×192K Board

General Description

The MEM86–3x192k memory board is a general purpose memory board that mounts in the Digital Reference Controller (DRC) rack and replaces up to three independent MEM86–192K memory boards. The board can be equipped with combinations of 32Kbyte Erasable, Programmable, Read Only Memory, (EPROMS) for firmware; 32kbyte CMOS–type Static Random Access Memory, (SRAM) for program storage; and 32kbyte Electrically Erasable, Programmable, Read Only Memory, (EEPROM) for program backup. Three configurations are actively supported for use in AB/S DRCs:

3100–MS4 DRC Basic Memory Board (MEM86–3*192/CMBMR3)

- CM 192kbyte EPROM Command Line Interpreter (CLIM)
- BM 192kbyte Block Memory (BLKM) and RAM
  - 64kbyte SRAM Stack and Data
  - 64kbyte EPROM Function Block Firmware
  - 64kbyte SRAM Program Storage (Groups 0 & 1)
- R3 192kbyte RAM Program Storage (Groups 2 –> 7)

3100–ME3 DRC Backup Memory Board (MEM86–3*192/E3E100)

- E3 192kbyte EEPROM Backup Memory (Groups 0 –> 5)
- E1 64kbyte EEPROM Backup Memory (Groups 6 & 7)
- 00 192kbyte empty sockets

3100–MS5 DRC Basic Memory and Backup (MEM86–3*192/CMBME2)

- CM 192kbyte EPROM Command Line Interpreter (CLIM)
- BM 192kbyte Block Memory (BLKM) and SRAM
  - 64kbyte SRAM Stack and Data
  - 64kbyte EPROM Function Block Firmware
  - 64kbyte SRAM Program Storage (Groups 0 & 1)
- E2 192kbyte RAM Program Storage and Backup
  - 64kbyte SRAM Program Storage (Groups 2 & 3)
  - 128kbyte EEPROM Backup Memory (Groups 0 –> 3)

Specifications

Power Consumption

		Bus	Battery
Equipped with CLIM+BLKM+RAN(MEM86–3* 192/CMBMR3)	+5V	1.2A	0.003mA
Fully equipped with EPROM–memories(27256)	+5V	1.3A	0
Fully equipped with SRAM–memories	+5V	0.85A	0.0054mA
Fully equipped with EEPROM–memories(28256)	+5V	1.4A	0

Battery: Varta 100, DKO, 3.6V, 100mAH

Environment

Temperature:	0°C to 50°C
Humidity:	5 to 95% (non–condensing)

Memory Location

The memory is divided into 18 32kbyte individually mapped memories or groups, whose address areas are set by software. There are 18 separate map registers located in the I/O address space for setting these memory address areas. Because the board replaces three independent MEM86–192k boards there are microswitches for three independent I/O address areas.

Two memory circuits are required to provide the 16 bit word length for each mapped memory area. Each pair of circuits handle 64kbytes or two memory groups. The map areas are separated from one another by the most significant address bit (A14) of the memory circuit. Two memory address maps could select the same circuit, so map addresses in succession must have have their most significant address bits in different states.

Supply Voltage Supervision and Battery Backup

Although no voltage supervision exists on the board itself, the use of memory is inhibited if the /PWF (power fail) signal from the bus is not in the 1 state. The /PWF signal inhibits the operation of the memory selection signals in the 0 state.

Normally, each pair of low power CMOS SRAM circuits are connected to the DC battery on the board. The Ni–Cd battery is charged whenever power is applied to the board. The limiting factor concerning how long the battery will maintain the memory, is its self–discharge rate. This depends on the temperature of the battery and its age. The cooler the ambient, the better.

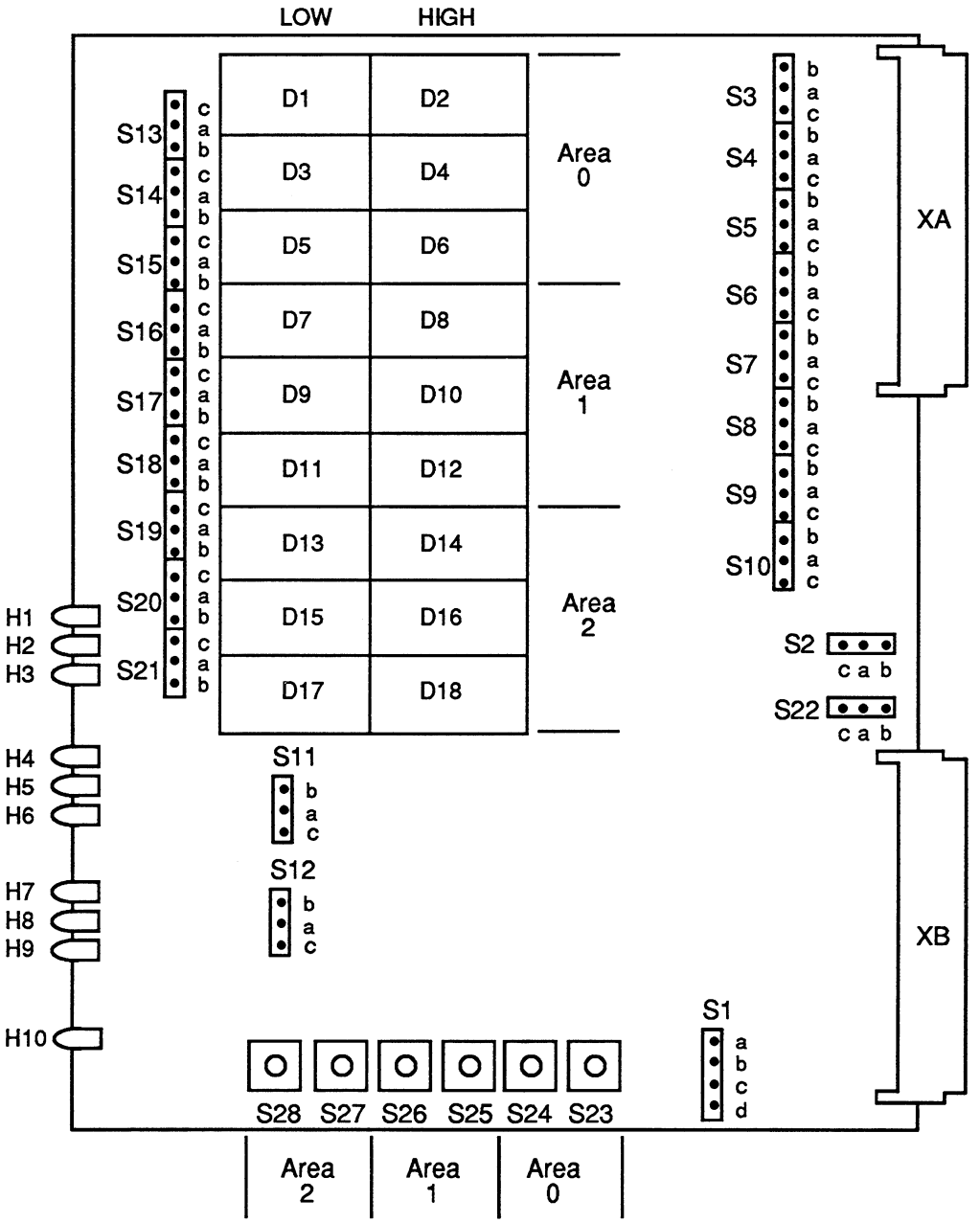
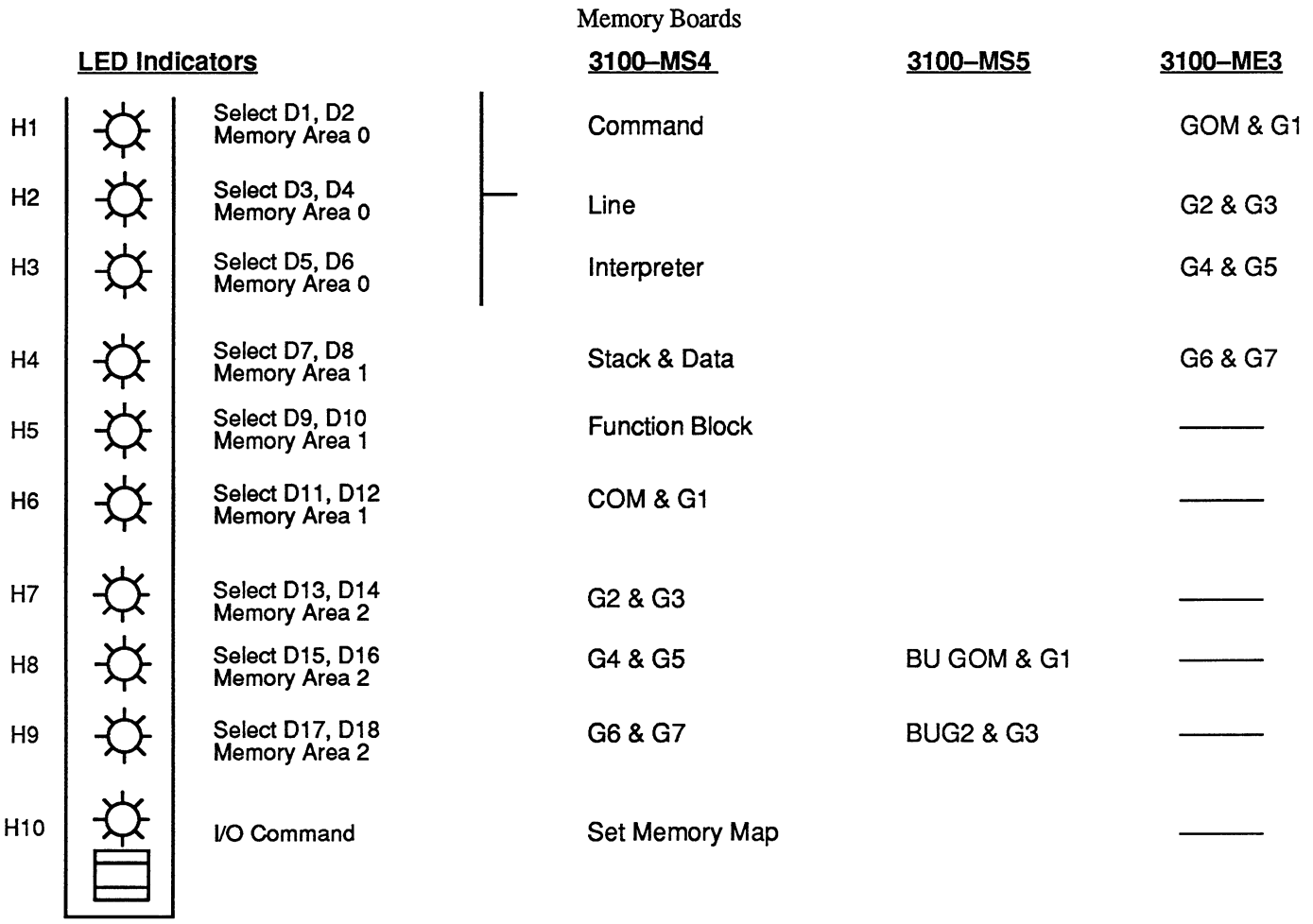


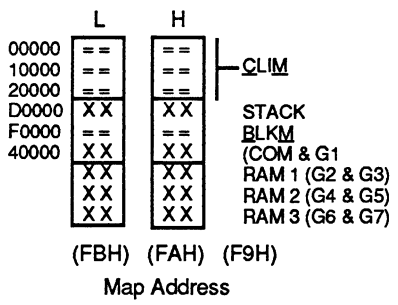
Figure 1. Component Layout



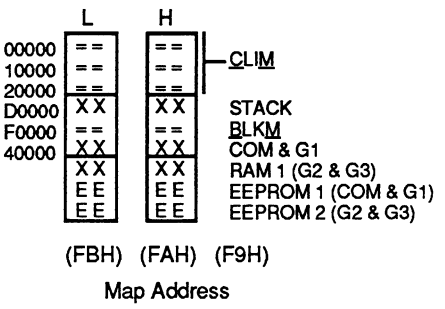
Location of Memory Circuits

== == = 16k byte EPROM

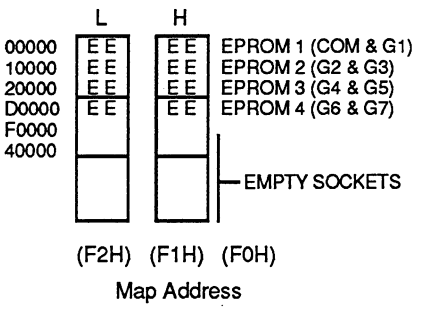
xx xx = 16k byte RAM



3100–MS4



3100–MS5



3100–ME3

Table 1. MEM Jumper Position and Switch Settings

Switch	Position	Purpose
S1	d–c* b–c a–b	No twait cycles One twait cycle Two twait cycles
S2	a–b* a–c	Secured power supply from the battery on the board, provided that S22 is in position a–b. Secured power supply from the bus (pins A30a, A30c)
S22	a–b* a–c	Battery connected (in use) Battery not connected
S3	a–b (ME3) a–c (MS4/MS5)	SRAM / EEPROM EPROM (D1 & D2)
S4	a–b (ME3) a–c (MS4/MS5)	SRAM / EEPROM EPROM (D3 & D4)
S5	a–b (ME3) a–c (MS4/MS5)	SRAM / EEPROM EPROM (D5 & D6)
S6	a–b (MS4/MS5/ME3) a–c	SRAM / EEPROM EPROM
S7	a–b (ME3) a–c (MS4/MS5)	SRAM / EEPROM EPROM
S8	a–b* (MS4/MS5/ME3) a–c	SRAM / EEPROM EPROM
S9	a–b* (MS4/MS5/ME3) a–c	SRAM / EEPROM EPROM
S10	a–b* (MS4/MS5/ME3) a–c	SRAM / EEPROM EPROM
S11	a–b* (MS4/MS5/ME3) a–c	SRAM / EEPROM EPROM
S12	——	Not Used
S13	a–b* (All) a–c	Circuits D1 and D2 voltage from +5V Circuits D1 and D2 voltage from battery
S14	a–b* (All) a–c	Circuits D3 and D4 voltage from +5V Circuits D3 and D4 voltage from battery
S15	a–b* (All) a–c	Circuits D5 and D6 voltage from +5V Circuits D5 and D6 voltage from battery
S16	a–b (ME3) a–c (MS4/MS5)	Circuits D7 and D8 voltage from +5V Circuits D7 and D8 voltage from battery
S17	a–b* (All) a–c	Circuits D9 and D10 voltage from +5V Circuits D9 and D10 voltage from battery
S18	a–b (ME3) a–c (MS4/MS5)	Circuits D11 and D12 voltage from +5V Circuits D11 and D12 voltage from battery
S19	a–b (ME3) a–c (MS4/MS5)	Circuits D13 and D14 voltage from +5V Circuits D13 and D14 voltage from battery

* Indicates normal jumper position.

Table 1. MEM Jumper Position and Switch Settings (continued)

Switch	Position	Purpose				
S20	a–b (MS5/ME3) a–c (MS4)	Circuits D15 and D16 voltage from +5V Circuits D15 and D16 voltage from battery				
S21	a–b (MS5/ME3) a–c (MS4)	Circuits D17 and D18 voltage from +5V Circuits D17 and D18 voltage from battery				
S23	LS	Setting of the addresses for map		MS4	MS3	MS5
			LSB	9	9	0
S24	MS	Registers of the area 0	MSB	F	F	F
S25	LS	Setting of the addresses for map		MS4	MS3	MS5
			LSB	A	A	1
S26	MS	Registers of the area 1	MSB	F	F	F
S27	LS RAM	Setting of the addresses for map		MS4	MS3	MS5
			LSB	B	B	2
S28	MS RAM	Registers of the area 2	MSB	F	F	F

* Indicates normal jumper position.

Normal Settings

Switch	Position	Purpose
S1	d–c	No twait cycles
S2	a–b	Secured power supply from the battery
S22	a–b	Battery connected
S3 through S11		Memory type (a–b = SRAM / EEPROM, a–c = EPROM) ME3 Always a–b
S12		Not Used
S13 through S21		Backup Voltage from (a–b = +5V, a–c = battery) EPROM a–b SRAM = a–c EEPROM a–b ME3 Always a–b
S23 through S28		Map addresses

Supply Voltage Supervision

Although no voltage supervision exists on the board itself, the use of memory is inhibited if / PWF signal (power fail) from the bus is not in the 1 state. The /PWF signal inhibits the operation of the memory selection signals in the 0 state.

Initial Jumper Positions and Switch Settings

XOYD ⟶ **3100–MS4**

S1 = D–C	S9 = A–B	S17 = A–B (256K Combined Memory)
S2 = A–B	S10 = A–B	S18 = A–C (MEM86–3x192K/CMBMR3)
S3 = A–C	S11 = A–B	S19 = A–C
S4 = A–C	S12 = N/A	S20 = A–C
S5 = A–C	S13 = A–B	S21 = A–C
S6 = A–B	S14 = A–B	S22 = A–B
S7 = A–C	S15 = A–B	
S8 = A–B	S16 = A–C	
S24 = F	S26 = F	S28 = F
S23 = 9	S25 = A	S27 = B

XOYD ⟶ **3100–MS5**

S1 = D–C	S9 = A–B	S17 = A–B (128K Combined Memory RAM/EE)
S2 = A–B	S10 = A–B	S18 = A–C (MEM86–3x192K/CMBME2)
S3 = A–C	S11 = A–B	S19 = A–C
S4 = A–C	S12 = N/A	S20 = A–B
S5 = A–C	S13 = A–B	S21 = A–B
S6 = A–B	S14 = A–B	S22 = A–B
S7 = A–C	S15 = A–B	
S8 = A–B	S16 = A–C	
S24 = F	S26 = F	S28 = F
S23 = 9	S25 = A	S27 = B

XOYD ⟶ **3100–ME3**

S1 = D–C	S9 = A–B	S17 = A–B (256K EE Backup)
S2 = A–B	S10 = A–B	S18 = A–B (MEM86–3x192K/E3E100)
S3 = A–B	S11 = A–B	S19 = A–B
S4 = A–B	S12 = N/A	S20 = A–B
S5 = A–B	S13 = A–B	S21 = A–B
S6 = A–B	S14 = A–B	S22 = A–B
S7 = A–B	S15 = A–B	
S8 = A–B	S16 = A–B	
S24 = F	S26 = F	S28 = F
S23 = 0	S25 = 1	S27 = 2

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