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Dynamic Overmodulation Characteristics of Triangle Intersection PWM Methods

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Abstract— **In this paper dynamic overmodulation characteristics of current regulated carrier based high performance PWM-VSI drives are investigated. Dynamic and steady state overmodulation operating modes are clearly distinguished, and the requirements for obtaining high performance in each mode are shown to be significantly different. Dynamic overmodulation characteristics of the popular triangle intersection PWM methods are modeled and shown to be unique for each method. The study reveals Space Vector PWM (SVPWM) exhibits a minimum voltage magnitude error characteristic. It also indicates all the advanced triangle intersection PWM methods including SVPWM have limited dynamic overmodulation performance. To enhance the performance, an algorithm with superior performance is adapted from the direct digital PWM approach. Detailed induction motor drive simulations illustrate the deficiency of popular triangle intersection PWM methods and the performance gained with the new dynamic overmodulation algorithm.**

I. INTRODUCTION

Voltage Source Inverters (VSIs) are widely utilized in AC motor drive, utility interface, and Uninterruptible Power Supply (UPS) applications as means for DC ⇔ AC electric energy conversion. Shown in Figure 1, the classical VSI which has 8 discrete voltage output states, generates a low frequency output voltage with controllable magnitude and frequency by programming high frequency voltage pulses. Of the various pulse programming methods, the carrier based Pulse Width Modulation (PWM) methods are the preferred approach in most applications due to the low harmonic distortion waveform characteristics with well defined harmonic spectrum, the fixed switching frequency, and the implementation simplicity.

Carrier based PWM methods employ the "per carrier cycle volt-second balance" principle to program a desirable inverter output voltage waveform. The triangle intersection implementation technique [1] which is increasingly being implemented in digital hardware/software and the direct digital pulse programming technique [2] (always digital software) are the two main methods to match the inverter output voltage with the reference value. As shown in Figure 2, in isolated neutral type applications the triangle intersection method is often accompanied with a zero sequence signal injection technique to enhance the drive performance when compared to Sinusoidal PWM (SPWM). Figure 3 illustrates the modulation waveforms of the popular zero sequence signal injection PWM methods [3, 4]. In the direct digital PWM technique, summarized in Figure 4 the vector space concept aids the calculation of the inverter state time lengths providing the per carrier cycle volt-second balance. In this approach, the partitioning of the two inverter zero states (defined as $\zeta_0 = \frac{t_0}{t_0+t_7}$, and $\zeta_7 = 1-\zeta_0$) provides the necessary degree of freedom in obtaining high performance [5]. The popular direct digital PWM methods are shown in Figure 5 and their triangle intersection equivalents indicated [4].

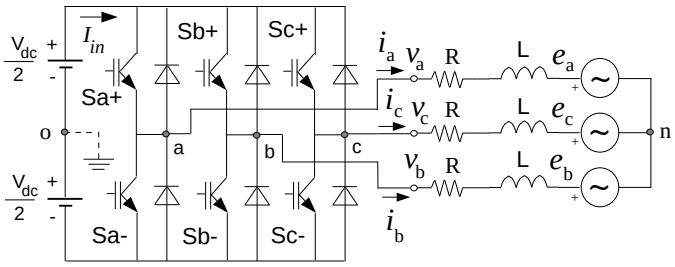

Fig. 1. Circuit diagram of a PWM-VSI drive connected to an R-L-E type load.

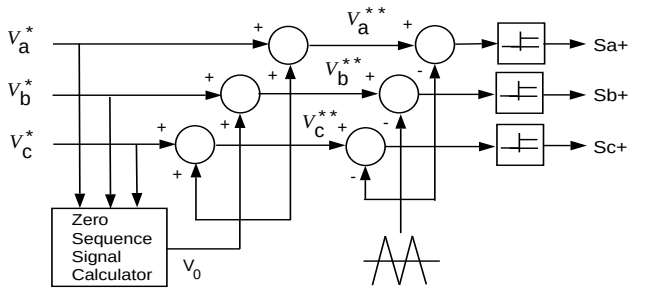

Fig. 2. The generalized signal block diagram of the triangle intersection technique based PWM employing the zero sequence injection principle.

In both the triangle intersection and direct digital techniques, the inverter voltage linearity is determined by the modulator characteristics. In the triangle intersection PWM technique, when the modulation signal magnitude becomes larger than the triangle peak value, and in the direct digital PWM technique when the reference voltage vector exceeds the inverter voltage hexagon boundaries, the voltage linearity is lost. With the exception of SPWM and THIPWM1/4, all the methods illustrated in Figure 3 and Figure 5 are linear in the $[0, 0.907]$ modulation index range ($M_i^* = \frac{|V^*|}{V_{1m6step}}$ where $V_{1m6step} = \frac{2V_{dc}}{\pi}$ and $|V^*|$ is the magnitude of the reference voltage vector). The SPWM method looses fundamental component voltage linearity at 0.785 modulation index, and THIPWM1/4 at 0.881 [6]. Outside the linearity range, the ratio of the output voltage fundamental component to its reference value is less than unity. This ratio, the voltage gain (G), rapidly decreases towards zero as the six-step mode is approached. Furthermore, the inverter output voltage contains substantial subcarrier frequency harmonics and drive performance degrades considerably [6]. The overmodulation range fundamental component voltage gain and waveform quality characteristics of the popular PWM methods, which are important for open loop (volts-per-hertz) controlled AC motor drives, are well understood [6, 7, 8].

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High performance AC motor drive and utility interface applications require closed loop current control algorithms with superior dynamic performance characteristics (in addition to the high steady state performance). Shown in Figure 6, the Synchronous Frame Current Regulator (SFCR) is the industry standard high performance current control algorithm. Although the linear modulation range performance of the SFCR meets the requirements in most applications, in the overmodulation region the drive performance significantly degrades, and bandwidth is lost [7, 9, 10, 11, 12]. Therefore, the steady state operation of the high performance PWM-VSI drives is confined to the linear modulation range. However, operation in the overmodulation region is allowed during transients and in the so called "dynamic overmodulation" region the full voltage capability of the modulator is utilized to improve the dynamic response. For example, in an induction motor drive, the speed response and robustness to load torque variations and disturbances can be greatly improved. Since the duration of the transients can be smaller than the maximum fundamental cycle, the per fundamental cycle modulator characteristics are not appropriate for the investigation of the dynamic overmodulation behavior of a modulator, and the per carrier cycle voltage linearity is important. The dynamic overmodulation characteristics of various direct digital PWM methods were investigated in [10, 22, 23] and various solutions with performance and implementation complexity trade-offs have been developed. The dynamic overmodulation characteristics of the triangle intersection PWM methods of Figure 3, however, have not been reported and their behavior is not well understood.

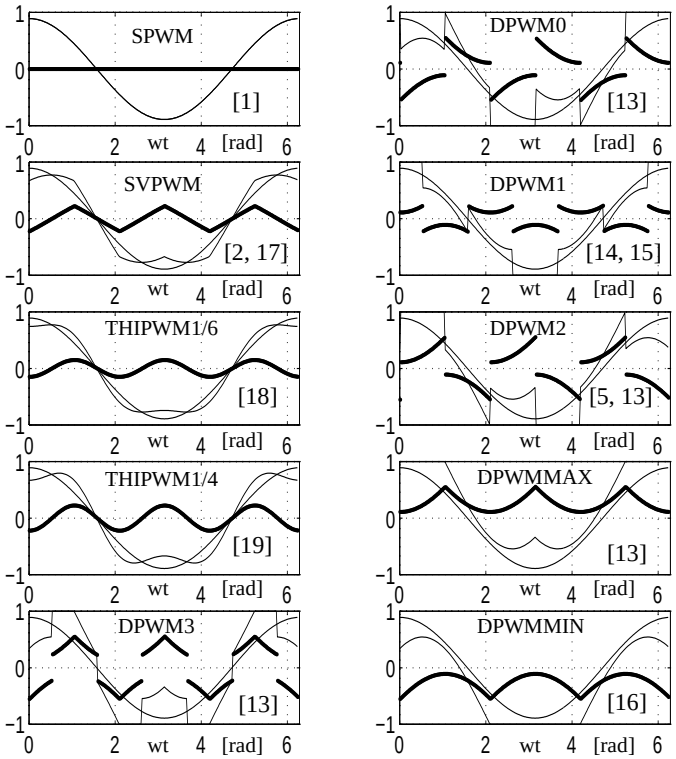

Fig. 3. Modulation waveforms of the popular PWM methods ($M_i = 0.7$).

This paper investigates the dynamic overmodulation characteristics of the popular triangle intersection PWM methods. The first section reviews the direct digital PWM dynamic overmodulation methods. In the second section the dynamic overmodulation characteristics of the popular triangle intersection PWM methods are analyzed in detail. Following the discussion on the influence of these characteristics on the drive performance in various applications, the induction motor drive behavior is investigated in detail and strong correlation is obtained between the theory and simulations.

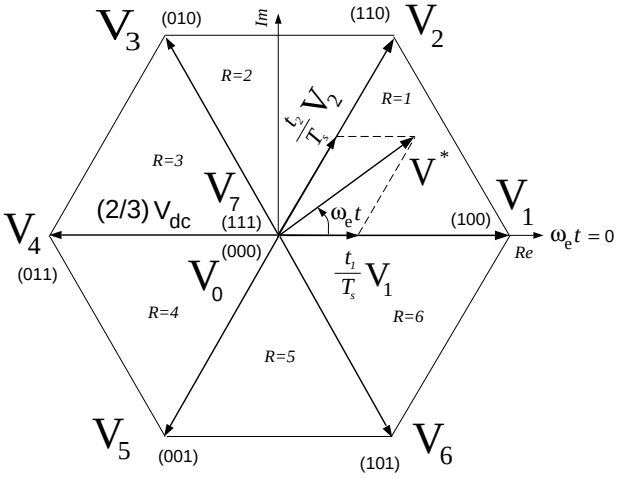

Fig. 4. The space vector diagram illustrates the direct digital implementation principle. The upper switch states are shown in the bracket as (Sa+, Sb+, Sc+) and "1" is "on" state while "0" corresponds to "off" state.

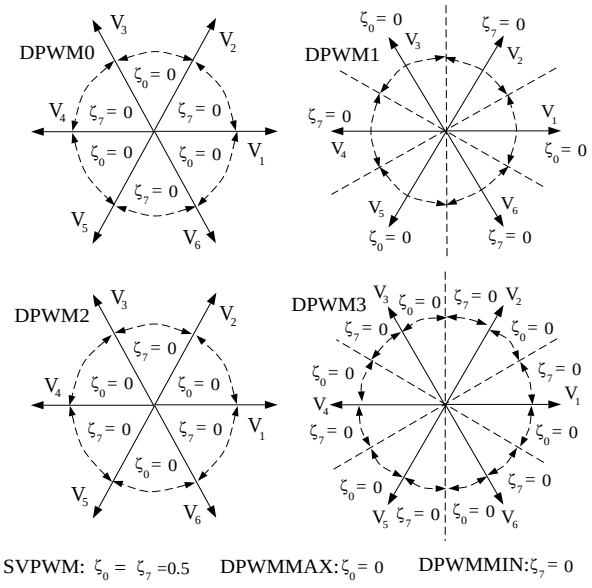

Fig. 5. Zero state partitioning of the popular PWM methods. DPWMMIN, DPWMMAX, and SVPWM have space invariant partitioning.

II. Direct Digital PWM Dynamic Overmodulation

In the space vector approach, employing the following complex variable transformation, the time domain modulation signals are transformed to the reference vector V^* which rotates in the complex coordinates at an angular speed $w_e t$.

$$V^* = \frac{2}{3}(v_a^* + a v_b^* + a^2 v_c^*) = V_{1m}^* e^{j w_e t} \quad where \quad a = e^{j\frac{2\pi}{3}} \quad (1)$$

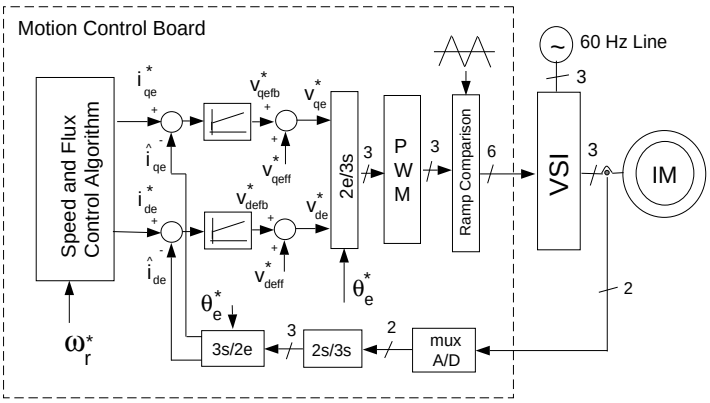

Fig. 6. High performance induction motor drive system diagram.

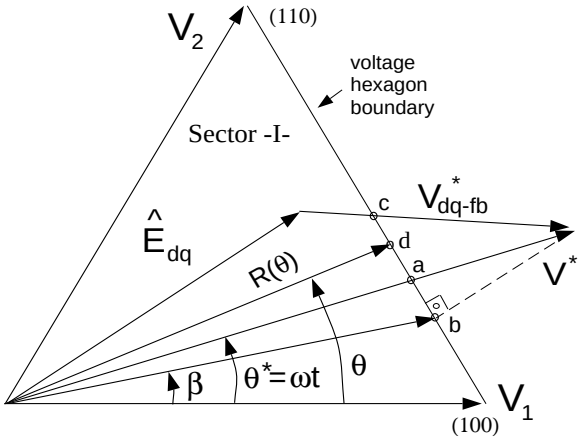

Fig. 7. Vector space illustration of the popular direct digital PWM technique dynamic overmodulation methods. a: minimum phase error method, b: minimum magnitude error method, c: dynamic field weakening method.

In the direct digital PWM technique, the complex number volt-second balance equation in the R'th sector of the inverter voltage hexagon in Figure 4 determines the time length of the two adjacent active inverter states R and $R+1$ ($R=6 \rightarrow R+1=1$) and the total zero state time length in the following [2].

$$V_R t_R + V_{R+1} t_{R+1} = V^* T_s \tag{2}$$

$$t_R = \frac{2\sqrt{3}}{\pi} M_i \sin(R\frac{\pi}{3} - w_e t) T_s \tag{3}$$

$$t_{R+1} = \frac{2\sqrt{3}}{\pi} M_i \sin(w_e t - (R-1)\frac{\pi}{3}) T_s \tag{4}$$

$$t_0 + t_7 = T_s - t_R - t_{R+1} \tag{5}$$

The zero state partitioning is decided by the programmer and typically a modulator among those shown in Figure 5 is selected with switching loss and waveform quality considerations [20]. Figure 4 indicates the per fundamental component voltage linearity of all the direct digital PWM methods is bounded by the circle which touches the inverter voltage hexagon and the per carrier cycle voltage linearity boundary is the hexagon. However, once the reference voltage vector tip point lies outside the hexagon, (5) yields a negative time length, hence an inevitable per carrier cycle volt-seconds error. A voltage vector on the hexagon boundary (the modified reference voltage vector) must be selected and at least one back step has to be taken to re-calculate the vector time lengths that generate the modified reference voltage vector. Shown in Figure 7, the three popular modified reference vector choices are the Minimum Magnitude Error PWM (MMEPWM) method (also called one-step-optimal method) [21, 22], the Minimum Phase Error PWM (MPEPWM) method [23], and the Dynamic Field Weakening PWM (DFWPWM) method [10, 11]. These methods were evaluated in [10, 11] for induction motor and AC Permanent Magnet (PM) motor drives. The superiority of the last method and the implementation simplicity of the second were shown.

In the triangle intersection PWM technique, unlike the direct digital PWM technique, the time lengths of the inverter states are not explicitly calculated: they are an end result of the comparison between the triangular carrier wave and the modulation waves. Therefore, an overmodulation condition can be detected when the modulation wave signal magnitude exceeds the triangle wave magnitude and switching ceases. The overmodulation intervals, i.e. the reference voltage vectors lying outside the modulator hexagon exhibit unique voltage error characteristics in each triangle intersection PWM method which will be analyzed in detail in the following section.

III. Triangle Intersection PWM Dynamic Overmodulation Characteristics

In the triangle intersection PWM technique, a reference voltage outside the triangle wave boundaries $\pm\frac{V_{dc}}{2}$ can not be generated. Modelling this saturation, dynamic overmodulation characteristics of any triangle intersection PWM method can be obtained. With this approach, by passing the reference modulation waves through the limiters shown in Figure 8 and employing transformation (1), as indicated in Figure 7, for any reference voltage vector $V_{dq}^* = \mid V_{dq}^* \mid e^{j\theta^*}$, an output voltage vector $V_{dq} = \mid R(\theta) \mid e^{j\theta}$ is produced. Since the zero sequence signals of all the popular modulation methods are symmetric and periodic, characterizing the first sector of the hexagon is sufficient. Since the hexagon boundaries are known, characterizing the angular relations, $\theta = f(\theta^*, M_i^*)$ is sufficient. For example, in the first sector $R(\theta)$ can be calculated by the following.

$$\mid v_{dq} \mid = R(\theta) = \frac{V_{dc}}{\sqrt{3}\sin(\theta + \frac{\pi}{3})} \tag{6}$$

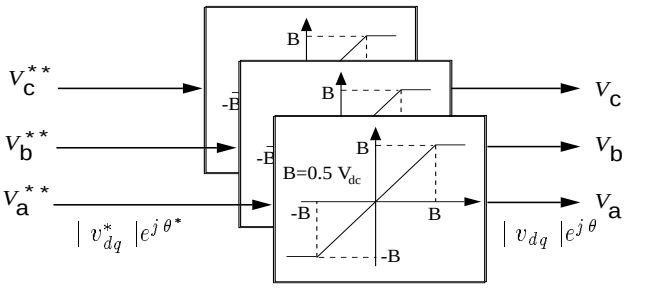

Fig. 8. The saturation block diagram of the triangle intersection PWM methods.

The dynamic overmodulation characteristics of the triangle intersection PWM methods shown in Figure 3 have been analyzed with the

above approach. The characteristics of SVPWM and the six popular DPWM methods are summarized in the following, while the SPWM, THIPWM1/4 and THIPWM1/6 characteristics are omitted and detailed analysis can be found in [9].

The triangle intersection implementation of SVPWM is possibly the earliest and simplest zero sequence injection PWM method developed [17]. This method employs the minimum magnitude test to determine the zero sequence signal. Assume $|v_a^*| \leq |v_b^*|, |v_c^*|$, then $v_0 = 0.5 \times v_a^*$. The analog implementation of triangle intersection SVPWM employs a diode rectifier circuit to collect the minimum magnitude signal from the three reference signals [17]. The digital implementation requires only three comparisons and a scaling to obtain this signal [24]. In either case, when the modulation signal becomes larger than the saturation boundaries $\pm\frac{V_{dc}}{2}$, the saturated modulation signals can be transformed by (1) and in the first segment ($0 \leq \theta^* \leq \frac{\pi}{3}$), the output voltage vector angle can be calculated in the following.

$$\theta_{SVPWM} = \arctan\left(\sqrt{3}\frac{1+\frac{6}{\pi}M_i^* cos(\theta^* - \frac{2\pi}{3})}{3-\frac{6}{\pi}M_i^* cos(\theta^* - \frac{2\pi}{3})}\right) \quad (7)$$

A software which graphically overlays the MMEPWM, and MPEPWM, and triangle intersection SVPWM dynamic overmodulation reference-output voltage vector trajectories indicated a surprising result: The MMEPWM and SVPWM vectors are exactly the same. Calculated by projecting the tip point of the reference voltage vector on the hexagon side (point b in Figure 7), the analytical angle relation of MMEPWM yields the following formula.

$$\theta_{MMEPWM} = \beta = -\frac{\pi}{3} + \arctan\left(\frac{\pi}{2\sqrt{3}M_i^* cos(\theta^* + \frac{\pi}{3})}\right) \quad (8)$$

Although (7) and (8) are different in form, their numerical evaluation which is shown in Figure 9 reveals the fact that their performance is the same. This result indicates when implemented with the triangle intersection technique, the SVPWM method provides very fast (one step optimal) dynamic overmodulation response. The MMEPWM methods employed in practice are complex and computationally involved [21, 22]. The triangle intersection SVPWM, however, can be implemented in hardware or software with minimum complexity.

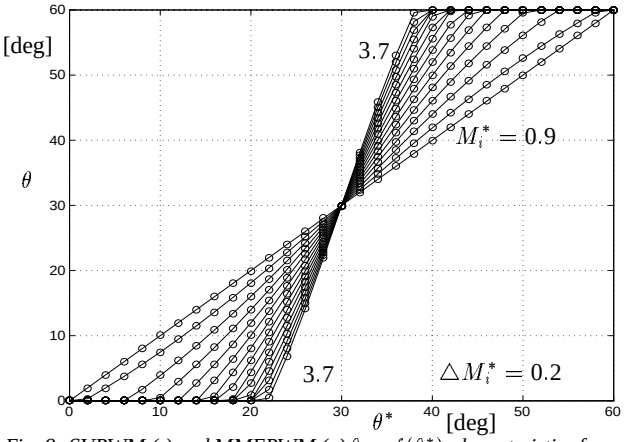

Fig. 9. SVPWM (-) and MMEPWM (o) $\theta = f(\theta^*)$ characteristics for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

The six popular Discontinuous PWM (DPWM) methods of which their waveforms are shown in Figure 3 have found application in high performance drives due to their low switching loss characteristics and low current ripple characteristics [3, 20]. Dynamic overmodulation characteristics of these modulators can be modeled depending on their zero state partitioning which was summarized in Figure 5. A zero state partitioning of $\zeta_0 = 1$, which corresponds to DPWM0 and DPWMMIN in the first hexagon sector, provides the following phase relations.

$$\theta_{DPWM0} = \arctan\left(\frac{\frac{6}{\pi}M_i^* \sin\theta^*}{2-\frac{2\sqrt{3}}{\pi}M_i^* \sin\theta^*}\right) \quad (9)$$

For DPWM2 and DPWMMAX the zero state partitioning in the first hexagon sector is zero ($\zeta_0 = 0$) and the dynamic overmodulation angle relations are calculated as follows.

$$\theta_{DPWM2} = \arctan\left(\sqrt{3}\frac{1-\frac{2\sqrt{3}}{\pi}M_i^* \cos(\theta^* + \frac{\pi}{6})}{1+\frac{2\sqrt{3}}{\pi}M_i^* \cos(\theta^* + \frac{\pi}{6})}\right) \quad (10)$$

Since in DPWM1 the zero state partitioning is $\zeta_0 = 0$ for $0 \leq \theta^* \leq \frac{\pi}{6}$ and $\zeta_0 = 1$ for $\frac{\pi}{6} \leq \theta^* \leq \frac{\pi}{3}$, the overmodulation phase relations are calculated from (9) and (10) in the following.

$$\theta_{\text{DPWM1}} = \begin{cases} \theta_{DPWM2} & 0 \leq \theta^* \leq \frac{\pi}{6} \\ \theta_{DPWM0} & \frac{\pi}{6} \leq \theta^* \leq \frac{\pi}{3} \end{cases} \quad (11)$$

The dynamic overmodulation characteristics of DPWM3 are found with the same approach in the following.

$$\theta_{\text{DPWM3}} = \begin{cases} \theta_{DPWM0} & 0 \leq \theta^* \leq \frac{\pi}{6} \\ \theta_{DPWM2} & \frac{\pi}{6} \leq \theta^* \leq \frac{\pi}{3} \end{cases} \quad (12)$$

The following phase error, $\triangle\theta$, definition aids the discussion on the modulator dynamic overmodulation characteristics.

$$\triangle\theta = \theta^* - \theta \quad (13)$$

The reference and output voltage vector phase relations of DPWM0, DPWM1, and DPWM2 are shown in Figures 10, 11, and 12 for various M_i^* values. In DPWM0 the output vector always leads the reference voltage vector while for DPWM2 the opposite is true. Since DPWM1 is a combination of DPWM0 and DPWM2, in this case the output vector lags the reference for the first 30° segment of the sector and leads in the following 30° segment. Note the phase error of SVPWM also changes polarity at 30°, however the change is smoother and the error magnitude is smaller. DPWM3 follows the opposite pattern of DPWM1 and both in DPWM1 and DPWM3 the output voltage vector experiences a jump near the midsection of the hexagon sector (avoiding the vector at $\frac{\pi}{6}$). For all the discussed methods the behavior in the first 60° is repeated periodically in the remainder of the sectors. In all the methods, an increase in the modulation index results in phase error increase and the error is the largest in DPWM1. Since the phase error completely determines the dynamic overmodulation performance of a modulator, the $\theta = f(\theta^*)$ (or $\triangle\theta = f(\theta^*)$)relations are the main characteristics in predicting the modulator dependent drive dynamic behavior.

In practice, the theoretical modulator linearity boundaries are further reduced due to the inverter blanking time and/or minimum pulse width constraint of the inverter drives [6]. If the narrow voltage pulses are eliminated, the output voltage magnitude becomes larger than the theoretical value and the phase error polarity is always opposite to theoretical modulator phase error polarity. The phase and magnitude errors are dependent on the minimum pulse width to the carrier cycle ratio and increase with it. Further detail on modeling these second order effects is reported in [9].

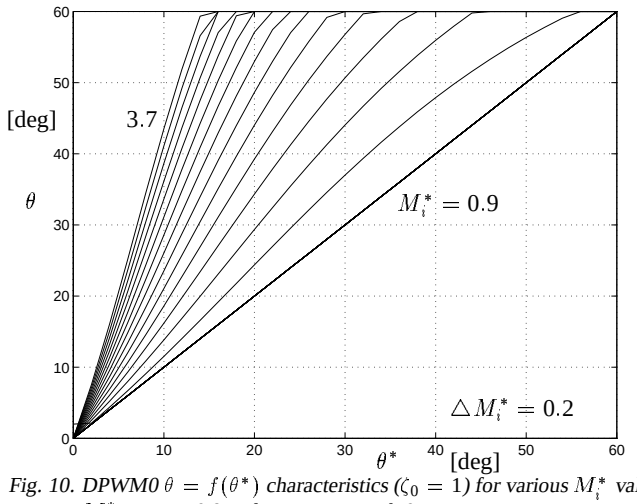

Fig. 10. DPWM0 $\theta = f(\theta^*)$ characteristics ($\zeta_0 = 1$) for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

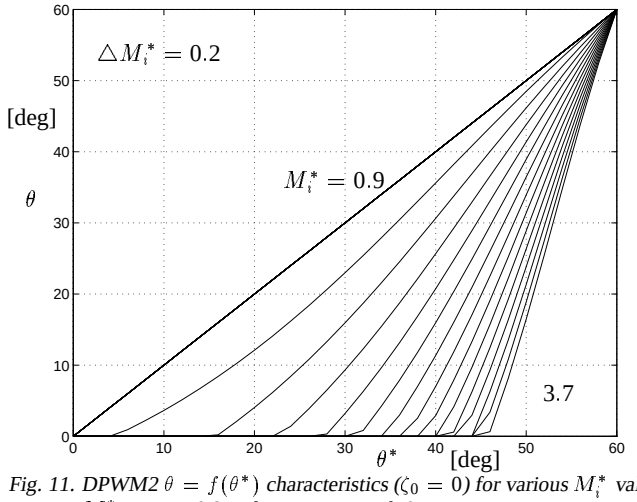

Fig. 11. DPWM2 $\theta = f(\theta^*)$ characteristics ($\zeta_0 = 0$) for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

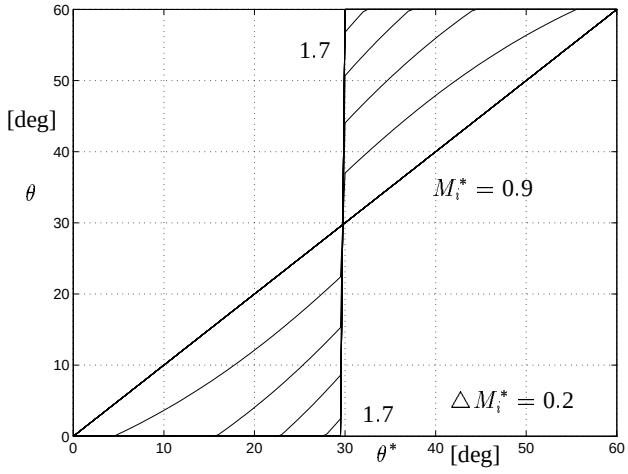

Fig. 12. DPWM1 $\theta = f(\theta^*)$ characteristics for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

IV. Drive Dynamic Overmodulation Behavior

The dynamic overmodulation performance of an AC motor drive or an AC line connected PWM-VSI is determined by the modulator phase error characteristics, the drive control algorithm, and load characteristics. In the following we first discuss the SFCR design, then investigate the system (SFCR-modulator-load) level overmodulation behavior.

Since the conventional SFCR design assumes modulator linearity, in the overmodulation region significant delays and overshoot can result. To minimize the performance degradation, antiwindup controllers which bound the integrator outputs of the Proportional Integral (PI) controllers are employed, and selecting a proper integrator limit value is vital in maximizing the dynamic performance [25]. An approach which selects SFCR integrator boundaries that keep the controller output signals on the edge of linearity was reported in [10, 11]. In this approach, shown in Figure 13, the SFCR discrete time signal flow diagram antiwindup limiters are only activated in the overmodulation region. During the (n)'th carrier cycle, the (n+1)'th cycle reference voltages v_{qe}^* and v_{de}^* are calculated and transformed to stationary frame *"abc"* variables. In the modulator block, a zero sequence signal is injected to the *"abc"* voltages to form the modulation signals. These signals are passed through the saturation limits of Figure 8 and rotated to the synchronous frame to predict the (n+1)'th cycle output voltages v_{qe} and v_{de}. If the reference and output signals are different (indicating a dynamic overmodulation condition), then the antiwindup signals reset the integrators to the boundary values ib_{qe} and ib_{de} (signal flow through "NL"), otherwise the linear modulation operating mode resumes (signal flow through "L"). In the overmodulation region, the "*d*" and "*q*" channel integrators are reset to $v_{qe}^* - v_{qe}$ and $v_{de}^* - v_{de}$ values so that in the following carrier cycle the calculated reference voltage vector is close to the hexagon boundary. With this approach, if the error reverses polarity, the linearity region is immediately reentered. If the error is zero or its polarity does not change, then the reference voltage remains near the modulator linearity boundary, however at a different point.

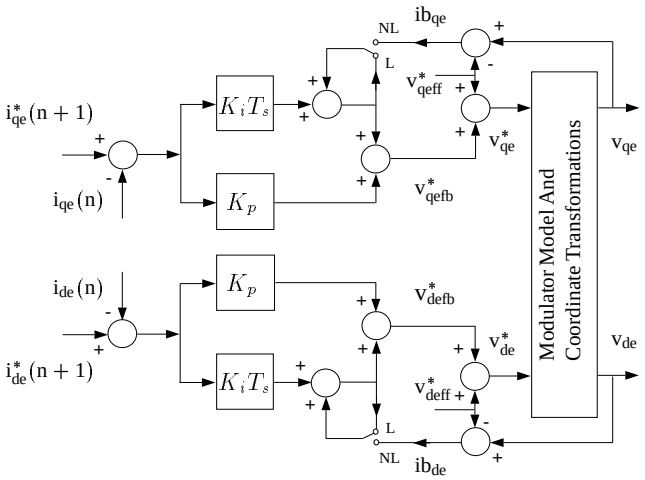

Fig. 13. Discrete time signal flow diagram of the synchronous frame PI current controller with anti-windup.

Along with the modulator and SFCR with antiwindup, the inverter DC voltage source and AC load characteristics define the system overmodulation behavior. Perhaps the most intuitive explation of the drive behavior is to consider the effect of the phase error on the synchronous frame reference and output voltage vector "*d*" and "*q*" components.

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Depending on the modulator phase error value, during a dynamic overmodulation condition the inverter output voltage vector may lead or lag the reference voltage vector, and the lead and lag conditions result in different "*de*" and "*qe*" axis voltages. As a result the drift of the "*d*" and "*q*" axis currents from the reference values may be quite different in the lagging and leading conditions. Therefore, the currents drift from the reference values according to the modulator phase error characteristics. For example, with SVPWM the drift always yields the smallest current error vector every carrier cycle and therefore SVPWM is suitable for applications where the inverter AC side current error minimization is of prime interest. However, in motion control systems the primary goal is to maintain the motion quality. A dynamic overmodulation condition implies an increase in the demanded torque and torque maximization is the prime concern. Since the torque maximization criteria and current error minimization criteria may require two different voltage vectors, the influence of the modulator phase error on the drive motor torque must be clearly understood. In this paper only the induction motor behavior will be discussed in detail and a study on other types of systems can be found in [9].

As shown in Figure 14, the rotor flux oriented synchronous frame induction motor steady state voltage vector diagram [26] indicates during overmodulation condition the "*qe*" and "*de*" axis stator voltages are different from the reference values and as a result the "*qe*" and "*de*" axis currents drift from their reference values. Thus, the motor torque linearity is lost ($T_e = K_{te}(i_{qse}\lambda_{dse} - i_{dse}\lambda_{qse})$) and motion quality degrades. For example, if v^*_{dqse}, v_{dqse} and the "*qe*" axis are in the first 30° segment of a hexagon sector, and v_{dqse} lags v^*_{dqse}, then the overmodulation condition results in a smaller v_{dse} and larger v_{qse} compared to the phase error lead condition. As a result i_{qse} becomes larger and i_{dse} smaller than the lead case. Although this dynamic field weakening condition may transiently increase the drive torque, motion quality degrades due to the loss of torque linearity. As the current regulation becomes poor and the field orientation condition is lost, the rotor flux varies and dynamics are excited. Beyond this point the dynamics can not be described with the steady state equivalent circuit of the motor drive; therefore a full dynamic model is required for a detailed investigation. However, the above discussed simple model illustrates the importance of the modulator phase error and also aids in explaining the influence of the phase lag and lead conditions. The most important conclusion of this intuitive example is that with a strong dynamic field weakening condition or the opposite effect the drive performance may significantly degrade. Therefore, the modulator phase error must be controlled in a manner to maintain good drive performance as much as possible.

Triangle intersection PWM methods exhibit unique phase error characteristics; therefore, it is expected that a drive perform differently with different modulators. Since the current controller antiwindup limiters bound the reference voltage magnitude (i.e. M_i^*), the phase error magnitude is also practically bounded. Thus, the antiwindup limiters are essential in avoiding unwanted dynamics. However, the antiwindup limiters may not be sufficient to obtain high performance (any motor torque is a strong function of the phase error and even a small phase error may result in a strong dynamic condition) and a system level study is required. In the following section, detailed induction motor drive simulations address these performance issues.

V. Computer Simulations

The theoretical modulator characteristic study has been supported by detailed induction motor drive simulations. A 5 HP, 1745 RPM, 460 V, 6.9 A, 4 pole induction motor with the lumped equivalent circuit parameters of $r_s = 1.97$ Ohm, $r_r = 1.73$ Ohm, $L_{ls} = L_{lr} = 11.2$ mH, $L_m = 275.6$ mH is driven through a PWM-VSI drive. The inverter DC bus voltage is 620 V, and the carrier frequency is 5 kHz. The drive employs an indirect field orientation control algorithm [26], and a fully digital synchronous frame PI current controller with voltage feedforward and antiwindup provides high performance current regulation [9, 24]. The digital current controller employs the synchronous sampling technique with 5 kHz sampling rate. The controller bandwidth is 250 Hz. The rated synchronous frame stator "*d*" and "*q*" axis currents are $I_{dseR} = 3.38$ A, and $I_{qseR} = 9.12$ A. The drive speed is controlled with a digital PI controller with antiwindup and the antiwindup limit equals the inverter maximum current capability. The speed controller sampling rate is 1 kHz and has a 25 Hz (electrical) bandwidth. The drive total inertia is $J_m = 0.05kgm^2$.

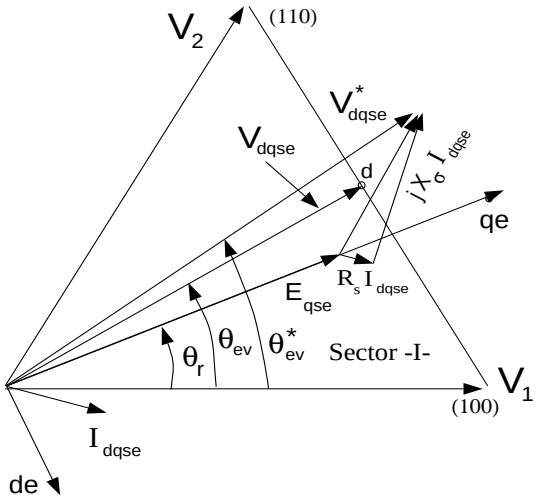

Fig. 14. Synchronous frame rotor flux oriented induction motor voltage vector diagram illustrated along with the inverter voltage vector diagram.

The computer simulations of Figure 15 to Figure 18 illustrate drive overmodulation performance with various modulators. While the drive is operating at 1500 RPM and no load, an overmodulation condition is generated with a speed reference change and application of a load torque. A speed ramp command, ω_r^*, at t=0.65 [s] increases the speed from 1500 RPM to 1600 RPM in 24 ms, and the load torque, T_L, increases at t=0.71 [s] from zero to 50% of the rated motor torque. Figure 15 illustrates the dynamics with SVPWM. The voltage vector phase error polarity and magnitude vary according to Figure 9. The current controller antiwindup channels keep the reference voltage vector near the hexagon boundary (M_i^* of (7) is kept small) and the SVPWM method selects a vector close to the reference vector (one-step-optimal) resulting in a small phase error. As Figure 15 indicates, SVPWM provides good performance.

Shown in Figure 16, the DPWM0 modulated system always has a negative phase error, consistent with the theoretical prediction. As the output voltage vector leads the reference voltage vector more than the SVPWM case, the field current experiences poorer regulation. Although results show an increase in torque and slightly better speed response, the oscillatory behavior can eventually result in a drive failure under certain operating conditions. Shown in Figure 17, the DPWM1

modulated system exhibits similar behavior to SVPWM, however its phase error magnitude is larger and the field current regulation capability degrades as in the DPWM0 case. Although DPWM1 has a substantially higher fundamental component gain than the other modulators [6], its dynamic performance is poorer than SVPWM. Therefore, it becomes clear that the open loop drive overmodulation performance criteria which suggests the modulator with the highest voltage gain is superior to the rest, and the closed loop system dynamic overmodulation performance criteria which suggests the modulator with the best speed response and disturbance rejection is superior to the rest, are different and result a in different modulator selection.

Shown in Figure 18, the DPWM2 modulated system simulations illustrate the dynamic overmodulation performance deficiency of this method. The phase error is large and always positive (lagging); the field current increases and results in reduced torque, hence very poor dynamics. Although in induction motor drive applications the linear modulation range switching loss characteristic of DPWM2 is superior to other modulators [20], its overmodulation performance is quite poor. Therefore, operation of this modulator in the overmodulation region should be prohibited or further control algorithm modifications are required.

The above simulation results indicate the SVPWM dynamic overmodulation performance is superior to all the other triangle intersection PWM methods. The modulator generates an output voltage vector with a small phase error and its one-step-optimal current regulation characteristic can successfully manipulate most dynamic conditions. However, very low inertia and very abrupt dynamic conditions could still not be properly manipulated and sufficiently large phase error intervals may result in unstable behavior and unacceptable drive performance. Therefore the modulator choice must be carefully made.

Since the above simulation studies suggest the DPWM methods have poor dynamic overmodulation characteristics and their large phase errors result in strong unwanted dynamics, when employing these modulators modifications to the drive control algorithm become inevitable. Since the DPWM methods have superior linear modulation range switching loss and waveform quality characteristics, a moderate increase in the control algorithm complexity and drive cost can be easily compensated with the performance gain. In this work two modification methods are suggested.

In the first approach, the DPWM method of choice is combined with SVPWM and when a dynamic overmodulation condition is detected, SVPWM is activated while in the linear region the DPWM method resumes control. Figure 19 illustrates the drive dynamic behavior with this algorithm. As the simulation waveforms indicate, in the linear modulation region DPWM2 is active, however as a dynamic overmodulation condition occurs the SVPWM signals are activated and the dynamics are rapidly manipulated. Since recent commercial drives often employ SVPWM and a DPWM method in combination to improve the linear modulation range waveform quality (for small M_i SVPWM and for large M_i DPWM is selected) and reduce switching losses [20], the modulation signal generating blocks may already exist in a drive and only an additional loop and re-calculation of the modulation signals is required. In particular implementing such an algorithm in a DSP based controller is an easy task.

In the second approach a more complex and higher performance algorithm, the dynamic field weakening method can be adapted from the direct digital technique [10, 11]. As shown in Figure 7, in this approach, the motor back EMF, $\hat{E}_{dqe}$, (calculated from the estimated stator flux) and the PI current controller outputs V^*_{dqefb}, are vectorially added and the intersection point with the hexagon (point "c" in the figure) is the tip point of the vector that forces the current error vector to move in the controller reference direction. By employing this algorithm, the reference voltage vector which is outside the inverter hexagon, is modified and returned to the inverter hexagon with a corrected phase such that any modulation method will exactly match the modified reference vector. Therefore, the modification algorithm performs equivalently with all the triangle intersection modulation methods. The simulation waveforms in Figure 20 illustrate the performance of DPWM2 combined with the dynamic field weakening method. When a dynamic overmodulation condition occurs, the dynamic field weakening algorithm is activated and the reference vector is modified and returned to the hexagon boundary such that DPWM2 exactly generates this vector. Note that this method generates a significantly small phase error and the field current experiences less transients than the SVPWM case. Also note the phase error alternates and during the speed ramp the field current increases for a short time interval. Due to this reason, a better term for the method would be "a phase error regulation method." This method however is fairly complex and requires substantial amount of calculations for relocating the reference voltage vector. Hence, only suitable for high performance fully digital drives with fast DSP controllers.

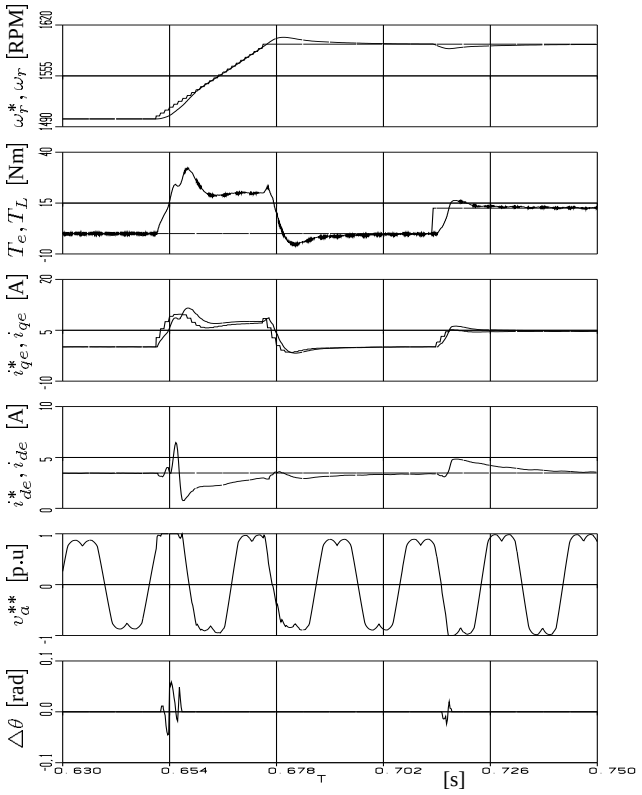

Fig. 15. Induction motor drive SVPWM dynamic overmodulation behavior under speed reference ramp change and load torque step change.

VI. Conclusions

Dynamic overmodulation and steady state overmodulation issues are different and the modulator fundamental gain characteristics are not a sufficient performance measure to evaluate the dynamic overmodulation performance. An elegant approach is the characterization of the reference and modulator output voltage vector angle and magni-

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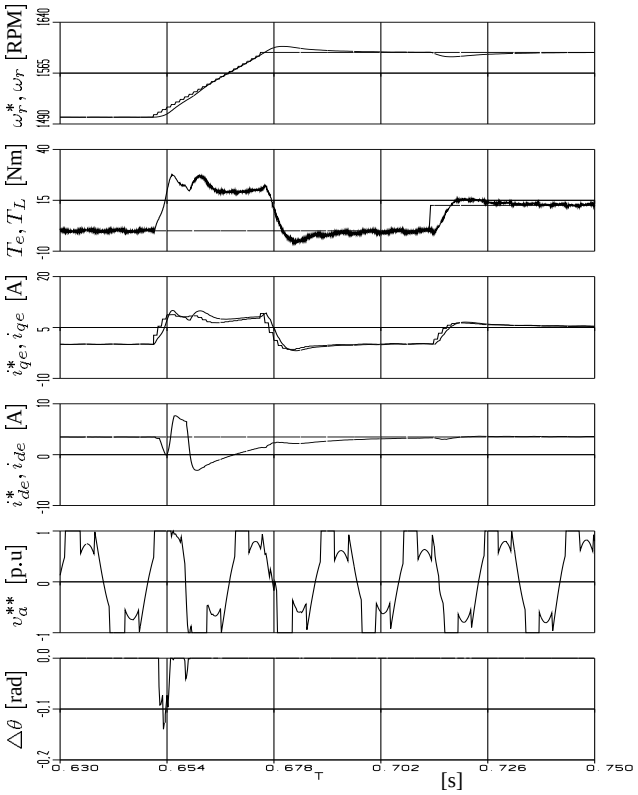

Fig. 16. Induction motor drive DPWM0 dynamic overmodulation behavior under speed reference ramp change and load torque step change.

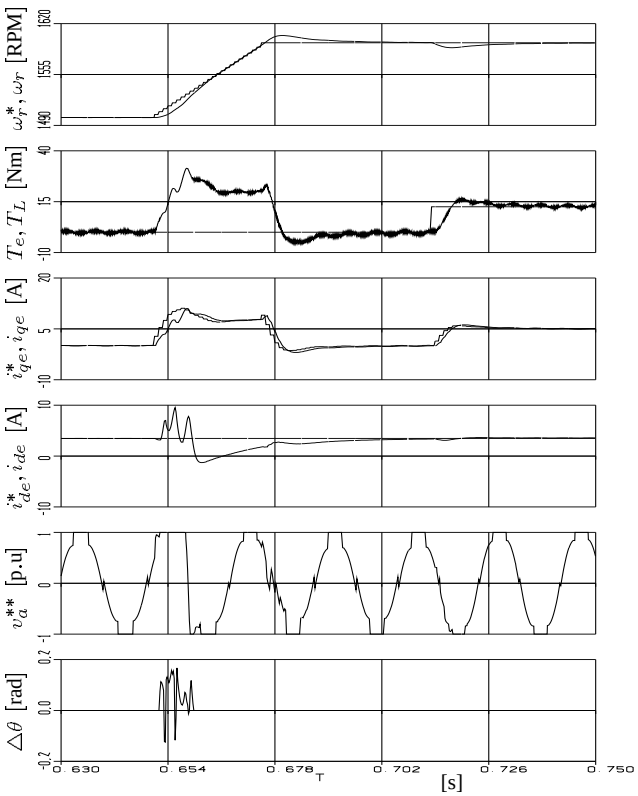

Fig. 17. Induction motor drive DPWM1 dynamic overmodulation behavior under speed reference ramp change and load torque step change.

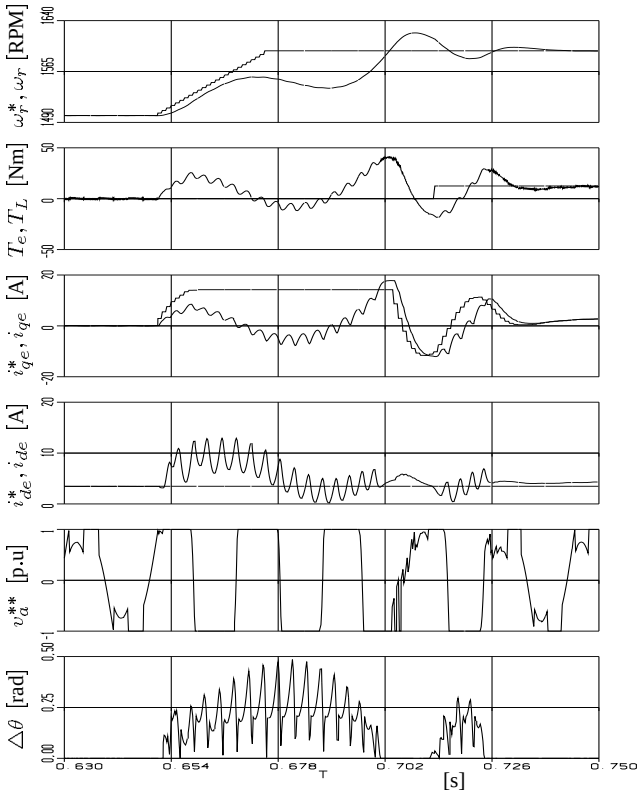

Fig. 18. Induction motor drive DPWM2 dynamic overmodulation behavior under speed reference ramp change and load torque step change.

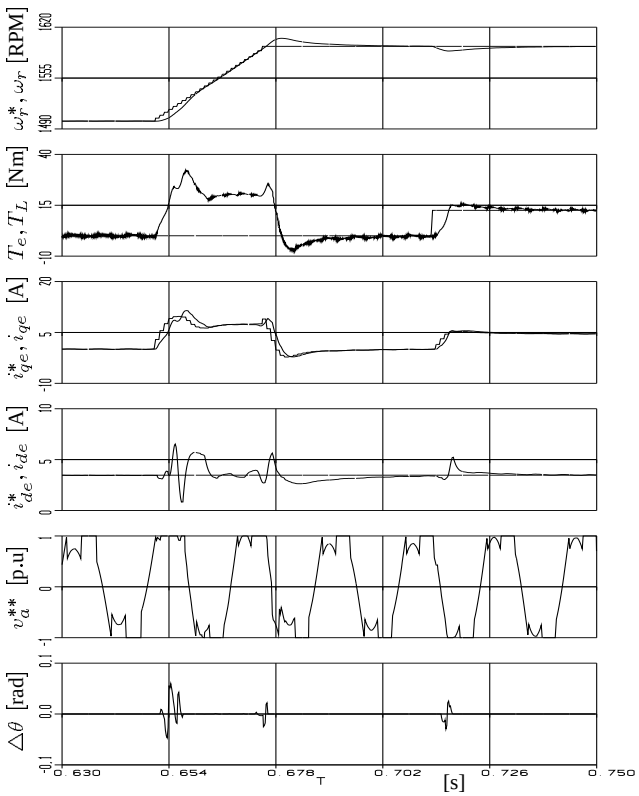

Fig. 19. Induction motor drive DPWM2 (linear mode) and SVPWM (overmodulation) combined algorithm dynamic overmodulation behavior.

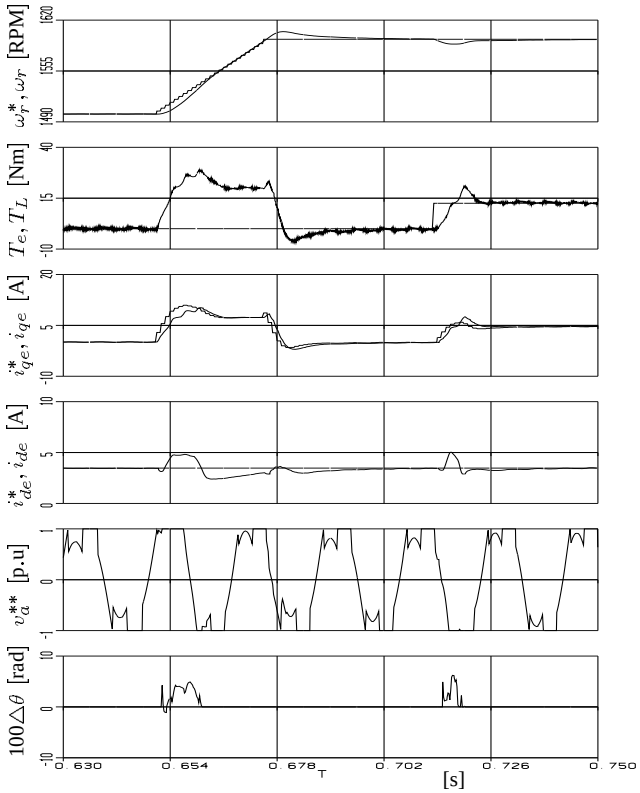

Fig. 20. Induction motor drive DPWM2 (linear mode) and DFWPWM (overmodulation) combined algorithm dynamic overmodulation behavior.

tude relations. A simple technique provides analytical tools to obtain these characteristics. Each triangle intersection PWM method is shown to have a unique dynamic overmodulation characteristic. The investigation reveals the minimum voltage magnitude error dynamic overmodulation attribute (one-step-optimal) of SVPWM method, indicating a significant implementation advantage compared to the two methods reported to achieve such performance. In a motor drive, motion quality is more important than rapid current control and the high performance phase error regulation approach is superior to the inherent overmodulation characteristics of the popular PWM methods. For intermediate dynamic overmodulation performance SVPWM provides satisfactory performance and for high dynamic overmodulation performance a phase error regulation method is adapted from the direct digital PWM technique to enhance the dynamic overmodulation characteristics of the triangle intersection PWM methods. In both methods the antiwindup limiters play an important role in keeping the phase error small and maintaining high dynamic performance. The theoretical modulator characteristics were verified by detailed computer simulations. The experimental work is in progress and will be reported shortly.

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